0.13 μm SiGe BiCMOS Technology Fully Dedicated to mm-Wave Applications

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***Abstract*—This paper presents a complete 0.13 μm SiGe BiCMOS technology fully dedicated to millimeter-wave applications, including a high-speed (230/280 GHz f_T/f_{MAX}) and medium voltage SiGe HBT, thick-copper back-end designed for high performance transmission lines and inductors, 2 fF/μm^2 high-linearity MIM capacitor and complementary double gate oxide MOS transistors. Details are given on HBT integration, reliability and models as well as on back-end devices models.**

***Index Terms*—BiCMOS integrated circuits technology, heterojunction bipolar transistor (HBT), integrated circuit fabrication, millimeter wave technology, Silicon Germanium (SiGe).**

I. Introduction

THE first STMicroelectronics technology capable of addressing the mm-wave domain was BICMOS9 with quasi self-aligned SiGe HBT reaching f_T/f_{MAX} values of 160/160 GHz [1]. As latest example, 24 GHz automotive radar circuits were successfully designed using this platform [2]. However, higher device performance is required to meet the needs of circuits operating at frequencies > 50 GHz and targeting 77 GHz automotive radars, 60 GHz WLAN, 100 Gb/s optical communications or non-intrusive imaging technologies [3], [4]. Moreover, the large cut-off frequency should not come at the expense of noise performance. This paper is an extension of the abstract published in the proceedings of the 2008 BCTM [5] and presents a 0.13 μm SiGe BiCMOS technology combining: i) an HBT architecture fully self-aligned thanks to the selective epitaxy of the SiGeC base (FSA/SEG) chosen for its high HF performances as well as record noise figures [6], and ii) a dedicated double thick-copper back-end for minimal line attenuation. We detail here this technology dedicated to mm-wave applications including high-speed (HS) and medium-voltage (MV) SiGe HBTs with RF-adapted passives, additional to 0.13 μm dual gate oxide CMOS and n-MOS varactors. HBTs integration, reliability, noise and model are discussed. Electrical parameters for other front-end and back-end devices are presented as well as the first results on integrated circuit using this technology.

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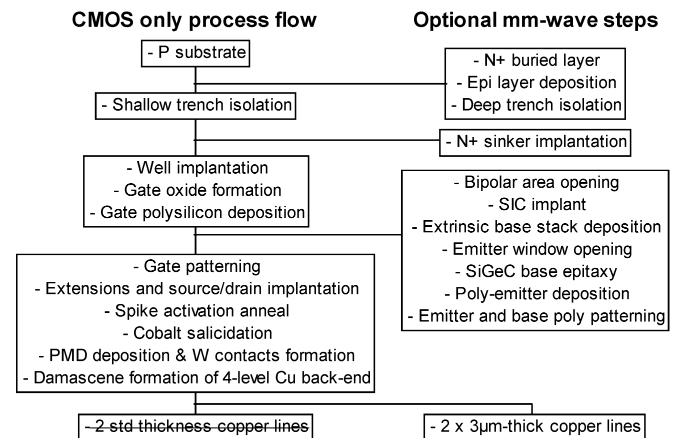

Fig. 1. 0.13 μm mm-wave technology integration scheme.

II. Technology Description

The general process flow for the BiCMOS technology is illustrated by Fig. 1 in comparison with the one used for a digital technology. The first part of the flow addresses the formation of the HBT collector with buried layer implantation, collector epitaxy and deep-trench formation. The shallow trench isolation is performed next and the wells for MOS devices are implanted in the Epi layer before gate oxide and poly gate deposition. The SiGe HBT emitter/base fabrication starts with the opening of the HBT region in the gate polysilicon and the implantation of the localized collector (SIC). The extrinsic base stack composed of oxide/poly/oxide/nitride is deposited as already described in [7]. The emitter window is etched in this stack and nitride sidewall spacers are formed to protect the extrinsic base polysilicon. A cavity is etched in the pedestal oxide for selective epitaxial growth of the SiGeC base connecting the extrinsic and intrinsic base and providing the full self-alignment of the E/B structure. The arsenic in-situ doped polysilicon emitter is deposited after D-shaped inside spacers formation. The HBT fabrication module ends by the patterning of the poly-emitter and the extrinsic base polysilicon protecting the MOS gate polysilicon during all the bipolar steps. In this integration scheme, the HBT module comes before the MOS source/drain formation to minimize the impact of the bipolar thermal budget—mainly due to the H_2 degas before SiGe epitaxy—on the MOS devices. As

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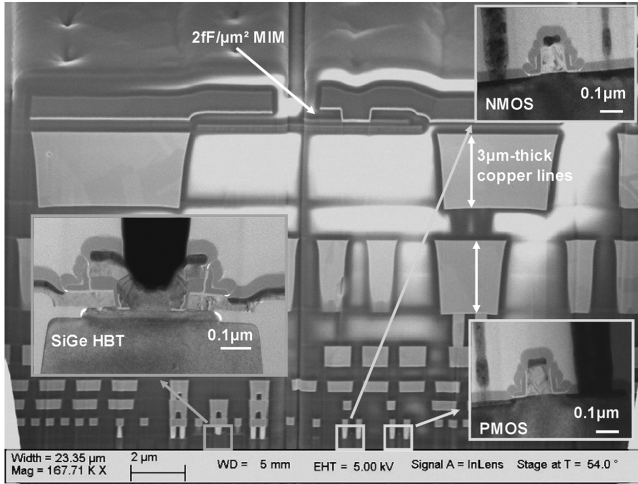


Fig. 2. SEM cross-section of the technology with thick-copper back-end, MIM capacitor and TEM pictures of the HBT and MOSFETs.

a result, CMOS spacers are also formed on poly-emitter sidewalls as can be seen in Fig. 3. A $\sim 1100\,^{\circ}$C RTP spike anneal is performed and cobalt is used for salicidation of active regions to end the front-end process steps. The interconnect lines are formed using a damascene process and made of six copper levels for which the two highest are 3-μm-thick (M5T and M6T). Finally, a 2 fF/μm^2 high linearity MIM capacitor is added and routed using the aluminum pad capping (Alucap) layer. Fig. 2 gives a cross-sectional view of the technology showing the three active devices, the MIM capacitor and the back-end interconnections.

III. Front-End and Back-End Devices Results

A. Compact Vertical SiGe HBT

In order to integrate the SiGe HBT in the BiCMOS technology, several modifications of the HBT-only process were required: i) the global device thickness was reduced to avoid photoresist thinning and dry etching issues during MOS gate patterning; ii) the vertical intrinsic profile was also thickened to accommodate dopant diffusion caused by the additional thermal budget due to CMOS integration. This last process modification led to an increase in the base transit time. In order to compensate for the performance loss due to f_T decrease, we changed the inner D-shaped spacer material from silicon nitride to amorphous silicon (α-Si) to reduce the device emitter resistance (R_E). Finally, a 20% reduction on R_E was obtained by topology reduction and an additional 30% decrease was gained by using α-Si for spacer formation. Fig. 3 shows the complete re-epitaxy of the amorphous material after the in-situ doped polysilicon emitter deposition which contributed to R_E improvement. As a consequence of R_E reduction, 20 GHz f_T/f_{MAX} improvement was measured on 0.12×4.85 μm^2 CBEBC devices (typical dimensions) despite little emitter/base capacitance (C_{EB}) increase. Thanks to the increase of the transit frequency on one hand and the optimization of the link between the poly-silicon extrinsic and the SiGe intrinsic bases to reduce base resistance and improve the maximum oscillation frequency, f_T/f_{MAX} values of $\sim$240/270 GHz were measured; approaching the technology target values for high-speed SiGe HBT devices of 230/280 GHz. Besides the high-speed HBT, a medium-voltage SiGe HBT can also be fabricated at no additional cost by protecting the device from SIC implantation. The collector-to-emitter breakdown voltage BV_{CEO} of such devices was raised from 1.56 V to 2.01 V. Maximum f_T dropped to 150 GHz and only little f_{MAX} reduction was observed due to concomitant base/collector capacitance (C_{BC}) reduction. Static and dynamic parameters for both types of SiGe HBTs are summarized in Table I.

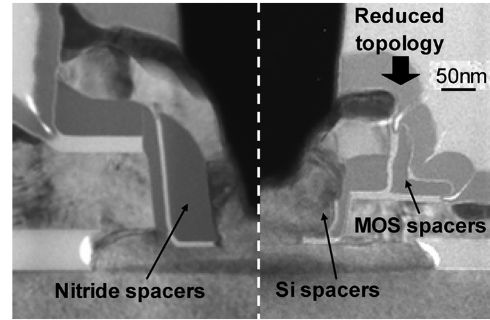


Fig. 3. TEM cross-sections illustrating the vertical SiGe HBT before (left) and after (right) integration in the BiCMOS flow.

TABLE I
STATIC AND DYNAMIC CHARACTERISTICS FOR HS AND MV SiGe HBTs WITH 0.12×4.85 μm^2 EMITTER AREA

Parameter	Unit	HS	MV	Comments
C_{BC}	fF	12.2	8.7	V_{CB}=0V
V_{BE} @ f_{Tmax}	V	0.91	0.84	
β @ f_{Tmax}		282	442	
BV_{CEO}	V	1.52	2.01	V_{BE}=0.7V
f_T	GHz	240	150	V_{CB}=0.5V
f_{MAX}	GHz	270	250	from f_{P20dB}

One of the most critical process aspects of self-aligned HBT devices regarding reliability is hot carriers trapping in the isolation between the emitter and the extrinsic base. We pointed out that, the use of re-crystallized Si as HBT spacers led to a great improvement in reliability relative to hot-carrier injection and mixed-mode degradation [8] by reducing carrier trapping after spacers re-crystallization. Electrical stress were applied and periodically interrupted for Gummel plot measurement using a parameter analyzer. In order to better illustrate the damage response, base current was measured at $V_{BE} = 0.5$ V. On forward mode (mixed-mode), transistors with 0.12×3.59 μm^2 emitter area were stressed by forcing a constant high current through the emitter with V_{CE} around (beyond) BV_{CEO} at room temperature. Various stress current levels were employed by taking nominal current density as a reference. Before starting our measurements, special care was taken in the stress setup to avoid device oscillations. Under a forward bias of 18 mA, the excess base current generated follows a stress time dependency given by $\Delta I_B(t) \propto t^n$—where t is the stress time. In our case, n was found to be close to 0.5 and the ideality factor of base current after stress around 2. These conditions describe a typical SRH

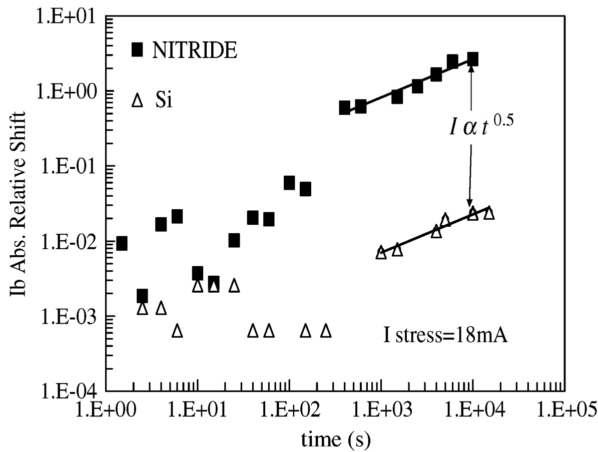
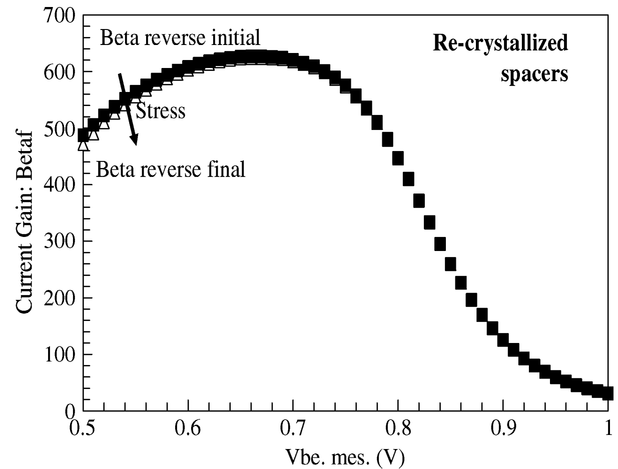


Fig. 4. Base current relative shift versus time under high forward current stress for HS HBT devices with nitride (squares) and Si (triangles) spacers (from [8]).

recombination across the major source of Generation-Recombination (G-R) centers: Si/SiO2 interface traps [9]. Fig. 4 emphasizes the good results obtained for devices with re-crystallized spacers showing that I_B degradation remained two decades lower than for devices using nitride spacers. Eventually, lifetimes higher than 10 years were extracted on the former devices. Investigations were also done under mixed-mode stress conditions with V_{CE} values of 1.8 V (higher than BV_{CEO}) and stress current of 28 mA. First results of degradation on reverse current gain displayed in Fig. 5 showed that devices with re-crystallized spacers where only slightly affected by such stress conditions contrary to devices with nitride spacers. As an additional illustration of the architecture robustness, Fig. 6 displays ideal I_B and I_C currents down to low V_{BE} on single and 10 K-transistor array (yield measured in-line was $> 90\%$ over 40 arrays of 3 K transistors).

Low frequency noise measurements were performed on HS and MV devices with length varying from 1 μm to 15 μm. The noise power spectra density (PSD) measured on typical HS devices are plotted in Fig. 7. PSD for both transistor types and all emitter lengths presented 1/f noise followed by shot noise. Extraction for base currents (I_B) in the range of 0.1 μA to 2 μA confirmed that the 1/f noise showed a quadratic dependence to I_B as generally observed [10]. The noise parameter K_b followed the classical $K_b = K_f \times A_E$ behavior where K_f is the noise level considering one emitter length and A_E the emitter window area. Similar noise parameters were extracted for the HS and MV devices family are, i.e., $Kb = 1.4 \times 10^{-10}$ μm^2 and 2.1×10^{-10} μm^2 respectively, which represents state-of-the-art results for SiGe HBTs [11]. Low frequency noise measurements on devices stressed under high forward current showed no degradation.

A complete model library has been developed for both HBT devices, which offers several Spice models simulation levels: the classical SGP (SPICE Gummel-Poon) model and the advanced HICUM model (Level2 or Level0 according to the choice of the designer). The library is "scalable" over a wide range of emitter lengths and allows the use of bipolar transistors with different configurations (multi-base, multi-collector, multi-finger). The main concern was to provide designers with



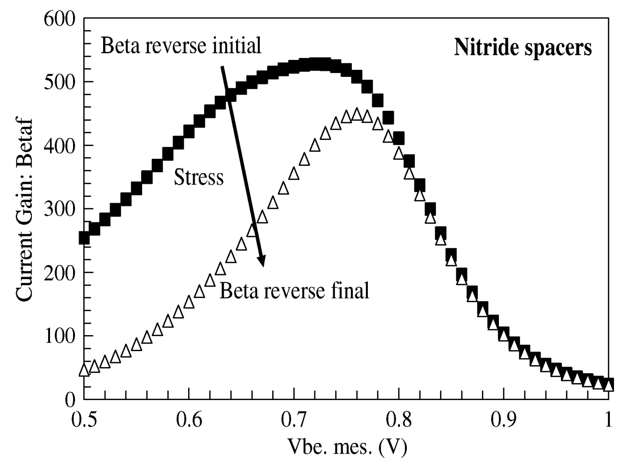


Fig. 5. Reverse current gain degradation versus emitter/base voltage V_{BE} for HS HBT devices before (squares) and after (triangles) stress under mixed-mode conditions (from [8], comparison between re-crystallized Si spacers on the top and nitride spacers on the bottom).

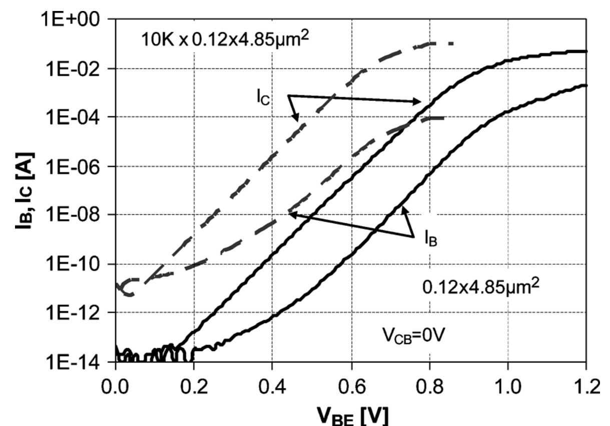


Fig. 6. Gummel plots measured on typical high-speed SiGe HBT and on yield structure after integration.

a model accurate and reliable for frequencies >50 GHz, in the range of mm-wave applications. As explained with details in [12], we used a smart and innovating methodology called "5-dummies" to de-embed the measurements and verify that the extracted model was representative of the intrinsic device and its first level of interconnect at high frequency. To demonstrate

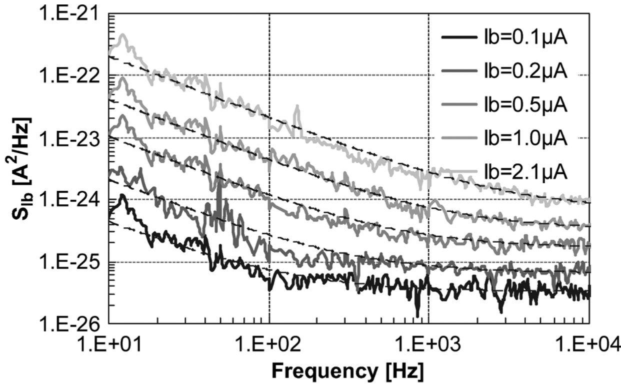


Fig. 7. Noise PSD for IB between 0.1 μA and 2.1 μA on typical HBT ($A_E = 0.12 \times 4.85\ \mu m^2$).

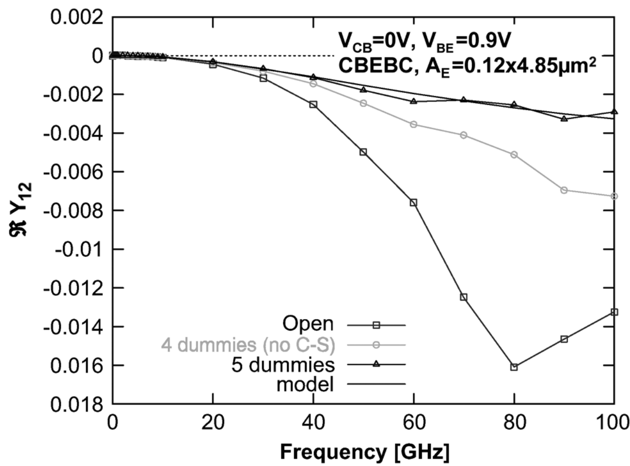


Fig. 8. $\mathrm{Re}(Y_{12})$-frequency, comparison of simulation («model» line) and measurements (line+dots) using 3 different methods for de-embedding.

the necessity of an accurate de-embedding for model/measurements matching verification, we took in Fig. 8 the example of the real part of [Y_{12}] and compared the model simulation with measurements using different de-embedding methods: i) the standard open; ii) the 4-dummies method with probe-short + pad-open + pad-short + regular-open de-embedding; and iii) the 5-dummies method adding the complete short. It is possible to verify that the model, extracted at 10 GHz, is representative of the device operating at mm-wave frequencies only if the de-embedding is correctly performed. It is clear in this figure that only the 5-dummies method allows correct model/measurements matching verification above 20 GHz. The self-heating description is also critical for model accuracy because these transistors—isolated with deep trenches—drive high current densities at high frequency. Thus, the self-heating phenomenon is accounted for in HICUM via a thermal sub-circuit with a resistance (R_{TH}) and a capacitance (C_{TH}) connected to the model thanks to a fifth thermal node. The R_{TH} and C_{TH} model is scalable as well in the Spice library. For a typical HS HBT device, Fig. 9 presents $f_T - I_C$ curves at growing V_{CB} together with a simulation of the temperature elevation in the device. The figure confirms that increasing the collector bias and the power dissipated in the device lead to an increase of the internal device temperature up to 50 °C at peak f_T for higher value of V_{BC}.

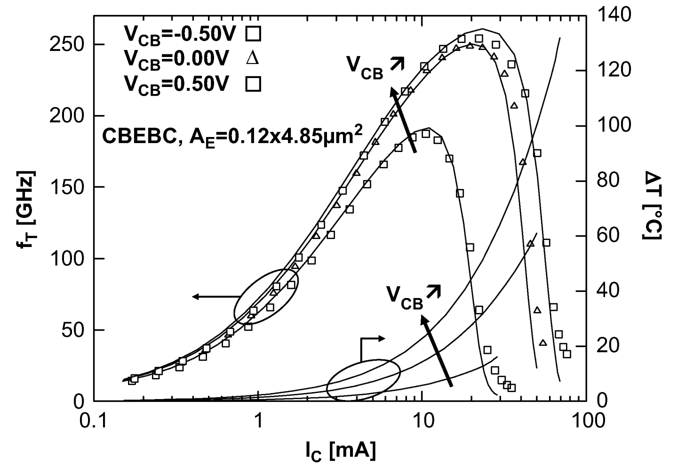


Fig. 9. $f_T - I_C$ at $V_{BC} = -0.5$ V, 0 V, 0.5 V, measurements (symbols) versus simulations (solid lines) for a typical HS HBT, simulated temperature elevation is plotted against the secondary axis.

Thanks to advanced de-embedding techniques and proper self-heating simulation, the model simulated all transistor geometries over a wide range of operation. For instance, Fig. 10 shows $f_T - I_C$ characteristics of transistors with emitter lengths between 0.85 μm and 14.85 μm. The accuracy of the model library is demonstrated from low to high injection, including f_T fall off. The drop of peak f_T for longer transistors usually observed on other models is compensated through accurate extrinsic resistances de-embedding. For short transistors, the correction of the model on f_T consists in better capacitances de-embedding. Regarding the dynamic behavior of the transistor model, it is also interesting to look at the Mason's Gain as figure of merit characteristic of the maximum oscillation frequency f_{MAX} of the HBT. Fig. 11 shows the Mason's Gain drop with the frequency up to 110 GHz at $V_{BC} = 0$ V, for a typical HS HBT. We note a very good correlation between the measurements and the model, even at peak f_T ($V_{BE} = 0.9$ V). As another [Y] parameters verification, we compare simulations versus measurements for the high-frequency noise figure of merit, NF_{min} calculated using a formulation combining measured currents, resistances and [Y] parameters described in [13]. In Fig. 12, the NF_{min} is correctly simulated, validating the accurate model of both DC and AC components and giving a good confidence in the HF noise model. We note here that state-of-the-art noise values are reached for our HS HBTs.

B. Double Gate Oxide MOS Devices

In addition to the SiGe HBTs, the technology also includes high-speed (HS) and low-leakage (LL) GO1 (2 nm) 1.2 V MOSFETs as well as GO2 (5 nm) 2.5 V MOSFETs from the 0.13 μm core CMOS developed at ST. As can be seen in Fig. 13, the devices fabricated using the BiCMOS flow without process tuning closely matched the core-process CMOS specifications thanks to our integration scheme minimizing the impact of the HBT thermal budget on the FET devices. The specifications were set using the 3σ dispersion of the device models, only fine tuning is therefore needed to re-center the devices parameters on the specification target. As a consequence, existing digital models for MOSFETs and derived devices can be used and digital libraries including MOS components and metal levels up to Metal3 are

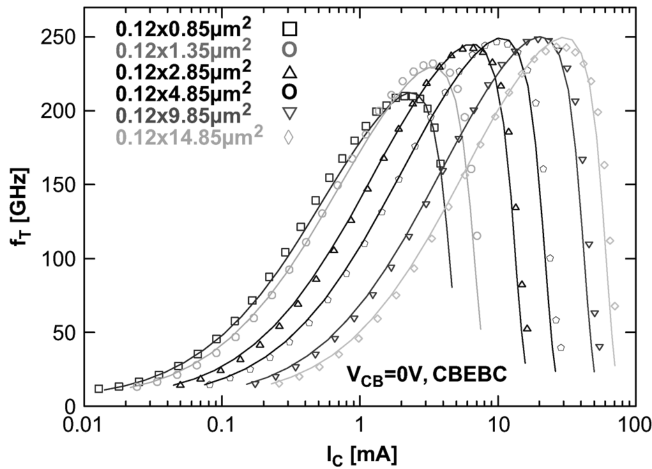


Fig. 10. $f_T - I_C$ for HS HBT devices with a wide range of emitter lengths, measurements (symbols) versus simulations (solid lines).

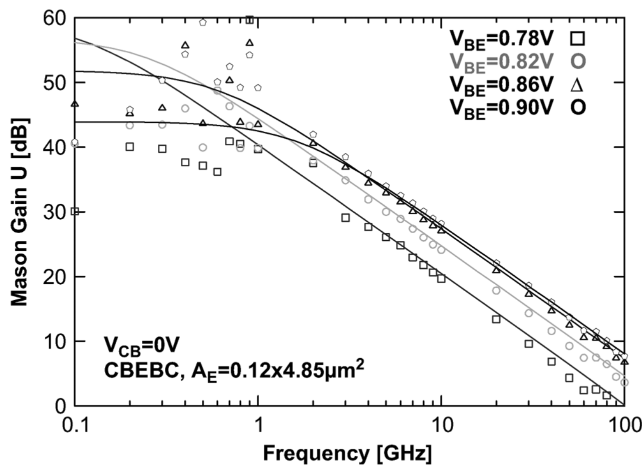


Fig. 11. U-frequency for typical HS HBT with V_{BE} between 0.78 V and 0.90 V and $V_{CB} = 0$ V, measurements (symbols) vs. simulations (solid lines).

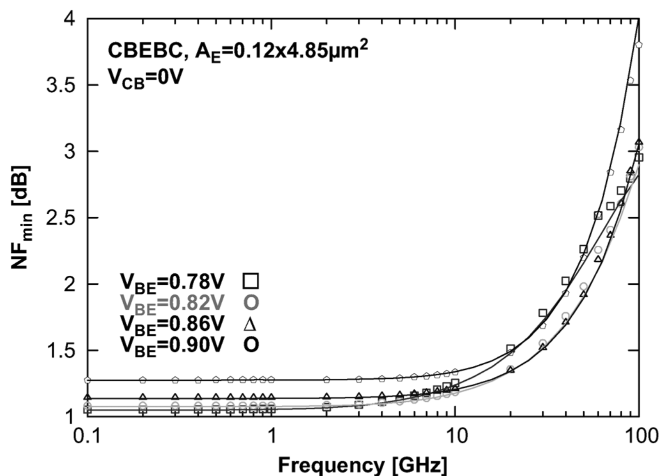


Fig. 12. NF_{min}-frequency for typical HS HBT with V_{BE} between 0.78 V and 0.90 V and $V_{CB} = 0$ V, measurements (symbols) versus simulations (solid lines).

directly portable. This insures easy design transfer of digital IPs from CMOS to high performance BiCMOS. Besides, accurate

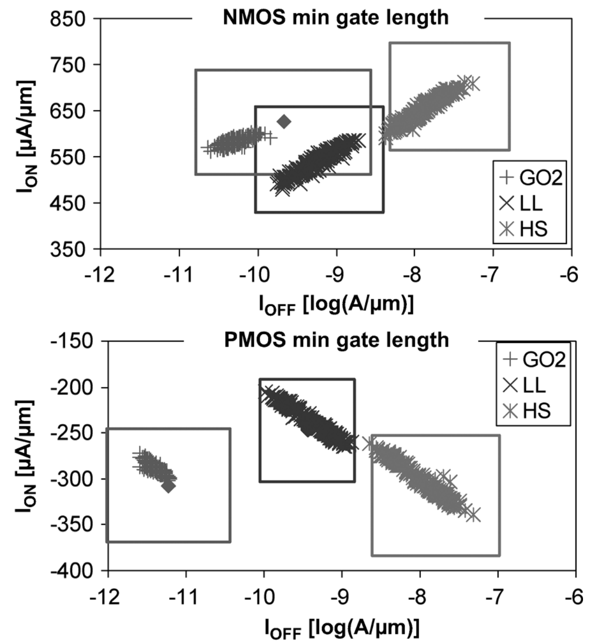


Fig. 13. $I_{ON} - I_{OFF}$ trade-off values (symbols) and 3σ model specifications (quadrats) for all 6 types of MOSFETs.

models up to 50 GHz were also developed for front-end analog devices.

Accumulation-mode n-MOS varactor test structures, using the thin gate oxide (2 nm), were also designed for operation in the 60–100 GHz range. For devices with minimum gate length of 130 nm and ten 1-μm wide gate fingers, the Q varies between 5 and 30 at 94 GHz, while the capacitance ratio remains close to 2, as illustrated in Fig. 14 and Fig. 15. The varactor diode presented in this work is optimized for the highest possible Q at mm-wave frequencies by using minimum gate length, thin oxide n-AMOS structures with 1 um wide gate fingers contacted on both sides of the gate. Experimental evidence obtained on n-type AMOS varactors fabricated in the 180 nm, 130 nm, 90 nm, 65 nm, and 45 nm nodes from different foundries and by different groups [14]–[17] has consistently shown that, for the highest Q, varactors must be designed with minimum gate length and minimum finger width. The latter generally increases the impact of the gate-bulk and gate-source overlap and fringing capacitance, somewhat reducing the CV ratio, to slightly below 2, when compared to structures with longer gates.

C. Back-End Process and Devices Results

As mentioned in the technology description, the back-end of the technology is made of six copper interconnection levels. Lines and inter-metal dielectrics (IMD) thicknesses were tuned to minimize signal attenuation and substrate coupling at high frequency. Two thick IMDs (1.5 μm) and copper lines (3 μm) top the copper interconnect and are fabricated using a single damascene process, the last copper layer lying 8.3 μm above the second metal level. Typical via resistance and line sheet resistance are lower than 0.8 Ω and 7 m$\Omega/\square$, respectively, and remain well within specifications, yield being >99% on 500 K via chains and >99.5% on 450 mm^2 metal combs.

Above the last copper level, the technology includes 2 fF/μm^2 MIM capacitors using Si_3N_4 as dielectric. Linearity

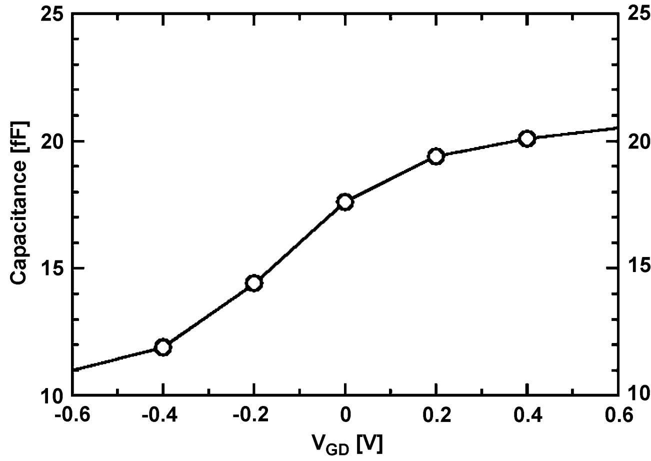


Fig. 14. n-MOS varactor capacitance versus bias voltage V_{GD} for gate area of $10 \times (0.13 \times 1.0)$ μm^2.

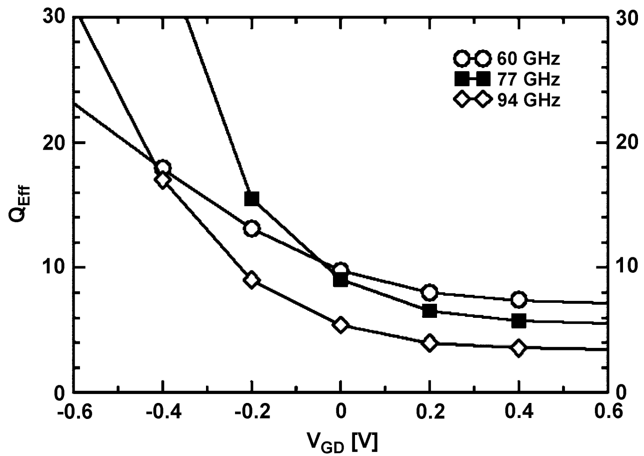


Fig. 15. Varactor Q values versus bias voltage V_{GD} for gate area of $10 \times (0.13 \times 1.0) \mu m^2$ at 60 GHz (circles), 77 GHz (squares) and 94 GHz (diamonds).

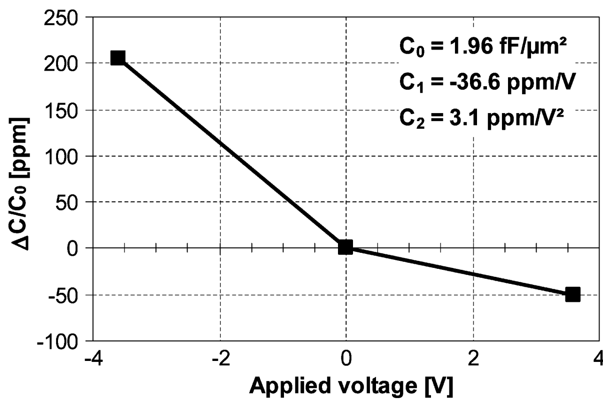


Fig. 16. Capacitance relative excursion versus applied voltage for 20 mm² MIM capacitors.

over the [−3.6 V, +3.6 V] range was monitored with in-line parametric test and is displayed in Fig. 16. Coefficient extraction is given at 25 °C for a $C = C_0 \times (1 + C_1 \times V + C_2 \times V^2)$ model. Other key parameters for the MIM capacitor are summarized in Table II together with results from microstrip lines and inductors described in the following paragraphs.

TABLE II
BACK-END DEVICES CHARACTERISTICS SUMMARY

Device	Charact. Value	Parameter	Comment
		0.40dB/mm	at 40GHz
Line	50Ω	0.50dB/mm	at 60GHz
		0.58dB/mm	at 77GHz
Induct. 1	74pH	Q = 25.2	at 60GHz
Induct. 2	107pH	Q = 24.0	at 77GHz
		C_0 = 1.96fF/µm²	at 25°C
MIM	39pF	Leak. <1nA/cm²	at -5V
		BV > 28V	at 25°C

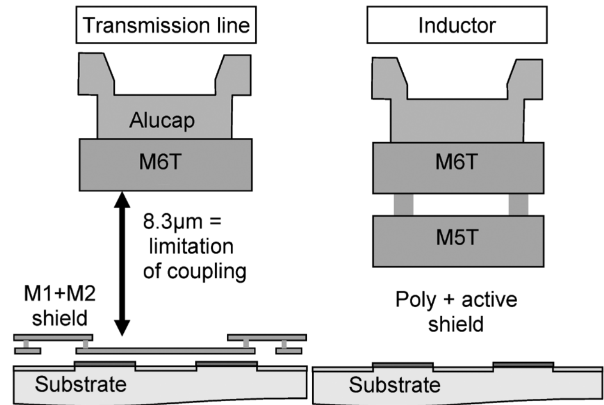


Fig. 17. Schematic cross-section of transmission lines and one-turn inductors using mm-wave back-end.

Microstrip transmission lines (T-lines) were laid out using 100% density wire made of M6T and Alucap layers and shielded vertically from the substrate by a mesh of the first 2 levels of interconnect in the shape of a grid due to CMP constraints (Fig. 17). The T-line characteristic impedance Z_C varied from 40.5 Ω to 71 Ω for widths between 20 and 4.4 μm with only little shift from 10 GHz up to 60 GHz as can be seen on Fig. 18. On-wafer measurements performed up to 110 GHz showed 0.5 dB/mm attenuation at 60 GHz on a 50 Ω characteristic impedance line. Attenuation values at other frequencies are displayed in Table II and plotted on Fig. 19. Phase velocities of these microstrip lines were fully linear up to 110 GHz and the propagation mode can be considered a quasi-TEM one.

1-turn octagonal shaped inductors using M5T, M6T and Alucap and shielded from the substrate were characterized and modeled. The cross-section of the device is illustrated in Fig. 17. Inductors using specific mm-Wave back-end have proved to have significantly higher Q values than inductors using digital back-end (Fig. 20). For 5 μm width inductors using specific back-end, the Q factor was measured on 74 pH and 107 pH devices respectively, showing maximum values of 25.2 at 60 GHz and 24.0 at 77 GHz respectively. The inductance model is scalable for values between 74 pH and 635 pH and frequency validity ranges from DC to the self resonance

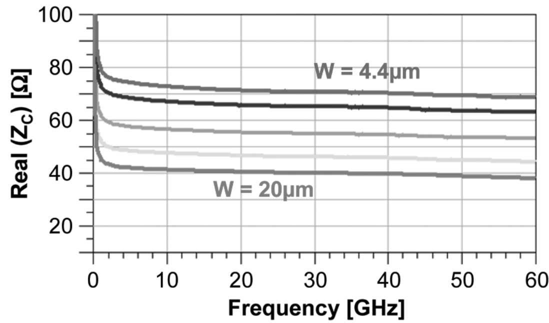


Fig. 18. Modeled impedance real value for microstrip lines with width between 4.4 μm and 20 μm.

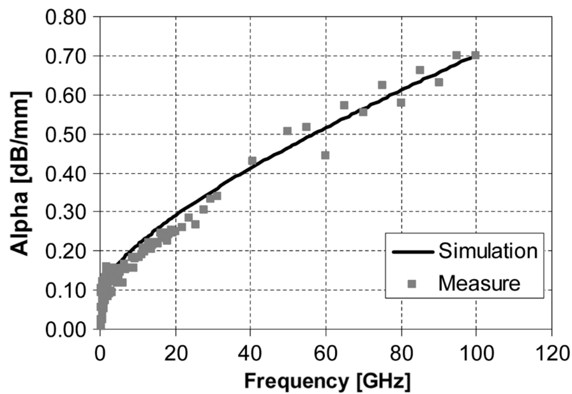


Fig. 19. Attenuation versus frequency μstrip Line ($\mathrm{W} = 11.5\ \mu\mathrm{m}$) of 51 Ω characteristic impedance.

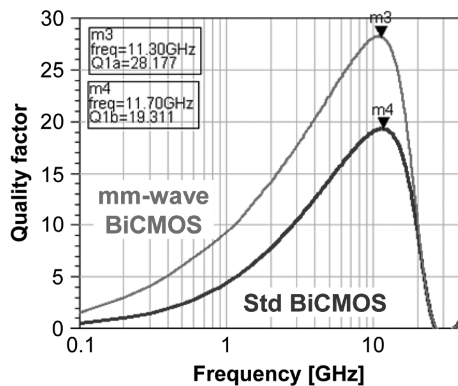


Fig. 20. Modeled Q factor versus frequency for 0.5 nH octagonal one-turn inductors using mm-wave and digital back-ends.

frequency (SRF) of the quality factor or 110 GHz if the SRF is greater than 110 GHz.

IV. Circuits Results

Finally, a 2.5 V 77 GHz receiver whose block diagram was transferred from the previous BiCMOS generation (Fig. 21) was fabricated using this technology before SiGe HBT full optimization i.e. with $\mathrm{f_T/f_{MAX}}$ values for the HS SiGe HBT reaching only 220/250 GHz [18]. The circuit included a 77 GHz VCO, a 3-stage LNA, doubly-balance Gilbert-cell mixer and IF-amplifier as can be seen in Fig. 22.

The total power consumption of the entire receiver was 123 mW, competing with 65-nm GP CMOS and a noise figure of 4.8 dB (vs. 7.5 dB for the CMOS circuit), 24 dB gain (versus 13 dB) and phase noise of −98 dBc/Hz (versus −95 dBc/Hz) at 1 MHz offset were achieved [19]. Other circuit characteristics are displayed in Table III below and more recent circuits will be presented elsewhere [20].

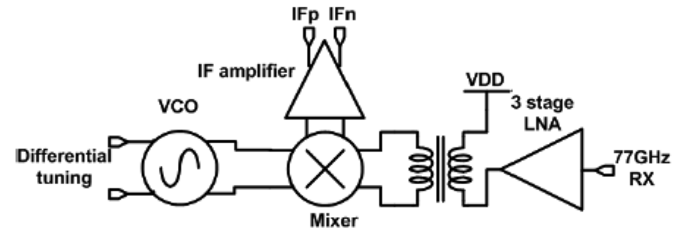


Fig. 21. Block diagram of the receiver transferred from previous BiCMOS technology.

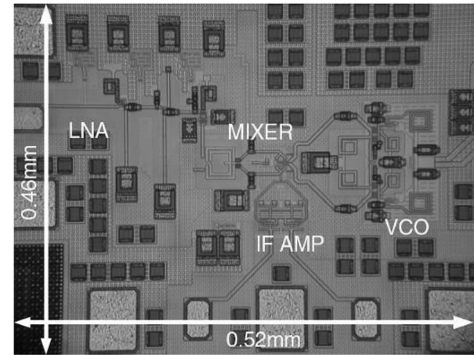


Fig. 22. Photograph of the receiver built using the mm-wave BiCMOS technology.

TABLE III
2.5 V 77 GHz SiGe BiCMOS Receiver Characteristics

RF/LO	Gain	NF	IP_{1dB}	P_{DC}	Area
77/76GHz	24dB	4.8dB	-22dBm	123mW	0.52x0.46μm^2

V. Conclusions and Perspectives

We presented in this paper a new 0.13 μm BiCMOS technology for mm-wave applications including high-speed and medium-voltage SiGe HBTs, dual gate oxide CMOS devices and specific back-end devices with full RF model offer. Integration of HS and MV HBTs was achieved with device performance reaching $\mathrm{f_T/f_{MAX}}$ values of 240/270 GHz for the HS device. Co-integration with dual gate CMOS was also successful as FETs are almost in specification with no additional work. The interconnect levels allowed 0.5 dB/mm attenuation at 60 GHz for 50 Ω microstrip lines and a quality factor of 24 at 77 GHz for octagonal shape inductors. Additionally, a 2.5 V receiver using non-optimized HS HBTs with power consumption similar to 65 nm CMOS reached record noise figure of 4.8 dB at 77 GHz.

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Julien Bouvier, photograph and biography not available at the time of publication.

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Sébastien Montusclat, photograph and biography not available at the time of publication.

Alain Margain, photograph and biography not available at the time of publication.

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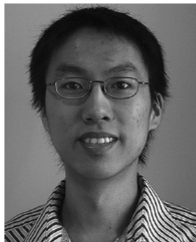

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