A Low-Voltage SiGe BiCMOS 77-GHz Automotive Radar Chipset

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***Abstract*—This paper presents a complete 2.5-V 77-GHz chipset for Doppler radar and imaging applications fabricated in SiGe HBT and SiGe BiCMOS technologies. The chipset includes a 123-mW single-chip receiver with 24-dB gain and an $IP_{1\,dB}$ of −21.7 dBm at 76-GHz local oscillator (LO) and 77-GHz RF, 4.8-dB double-sideband noise figure at 76-GHz LO and 1-GHz IF, and worst case −98.5 dBc/Hz phase noise at 1-MHz offset over the entire voltage-controlled oscillator tuning range at room temperature. Monolithic spiral inductors and transformers result in a receiver core area of 450 μm× 280 μm. For integration of an entire 77-GHz transceiver, a power amplifier with 19-dB gain, +14.5-dBm saturated output power, and 15.7% power-added efficiency is demonstrated. Frequency divider topologies for 2.5-V operation are investigated and measurement results show a 105-GHz static frequency divider consuming 75 mW, and a 107-GHz Miller divider consuming 33 mW. Measurements on all circuits confirm operation up to 100 °C. Low-power low-noise design techniques for each circuit block are discussed.**

***Index Terms*—Automotive radar, frequency dividers, low-noise amplifiers (LNAs), millimeter-wave imaging, millimeter-wave receivers and transmitters, power amplifiers (PAs).**

I. Introduction

SYSTEMS FOR W-band radar and millimeter-wave imaging are under development in the latest SiGe processes with f_T/f_{MAX} over 200 GHz [1] and in nanoscale CMOS. State-of-the-art demonstrations of silicon technology for W-band applications include RF circuit blocks at 77 GHz and above [2]–[18], 77-GHz receivers and transmitters [19]–[27], and transceivers [28], [29]. Recently, CMOS and SiGe HBT receivers and transceivers have even been pushed to operate at 95 GHz [30] and 160 GHz [31], respectively.

A receiver or transceiver array is required in imaging applications, making power consumption a critical concern. Although low-power 65-nm CMOS receivers have been demonstrated up to 95 GHz, reliable operation of the static frequency divider at 100 °C has yet to be accomplished [11], [17], [30]. While SiGe BiCMOS technology continues to maintain a performance advantage over CMOS in terms of gain, noise figure (NF), phase noise, and output power, especially over temperature, research to date using SiGe HBT technology is not focused on minimizing power consumption. Some 77-GHz SiGe HBT circuit blocks use sub-2.5-V supplies [2], [7], [9], [11], but existing millimeter-wave SiGe HBT receivers and transmitters operate with power supplies in the 3.3–5.5-V range. In particular, state-of-the-art SiGe HBT, GaAs, and InP frequency dividers require supply voltages greater than 3.3 V and consume over 100 mW [12]–[16].

This paper presents a low-power 2.5-V 77-GHz SiGe BiCMOS chipset for automotive and millimeter-wave imaging applications based on the work in [18]. The chipset contains all RF circuit blocks (voltage-controlled oscillator (VCO), low-noise amplifier (LNA), power amplifier (PA), down-conversion mixer, and frequency divider) required to fabricate a fully integrated 2.5-V 77-GHz transceiver with a phase-locked loop (PLL). Theoretical analyses of the circuit blocks focus on obtaining sufficient speed to operate at 77 GHz with low noise and minimal power consumption. The circuit blocks are characterized individually and proof of integration is demonstrated with a receiver containing the VCO, LNA, down-conversion mixer, and IF amplifier.

II. Transceiver Architecture and Circuit Blocks

A block diagram of a direct conversion transceiver suitable for Doppler radar is shown in Fig. 1, where boxes with dashed lines indicate the circuit blocks discussed here. Integration is demonstrated using a receiver with the architecture shown in Fig. 2, equivalent to the CMOS receiver presented in [24]. In a real system, the power dissipation of the IF amplifier could be reduced because it would not have to drive 50 Ω.

To further minimize power dissipation in massively parallel passive millimeter-wave imaging systems, such as those intended for 3-D biomedical applications and millimeter-wave cameras [32], only a portion of the receivers in the system are turned on simultaneously [33]. For example, a 100-kilo-pixel millimeter-wave camera would consume 5000 W at 50 mW/pixel. However, if only 100 pixels were "on" simultaneously, it would consume 5 W. At an equivalent shutter speed of 1/60 s, each set of 100 pixels would then have 16.7 μs to power up, stabilize, and image. The pixels could be turned on and off in such a manner as to minimize temperature gradients

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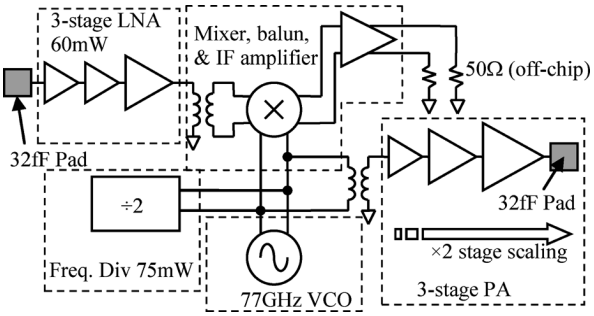

Fig. 1. 77-GHz Doppler transceiver architecture.

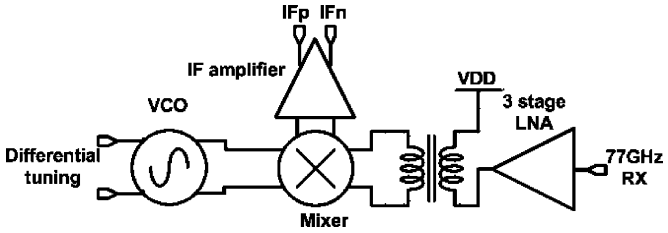

Fig. 2. Block diagram of a low-power receiver.

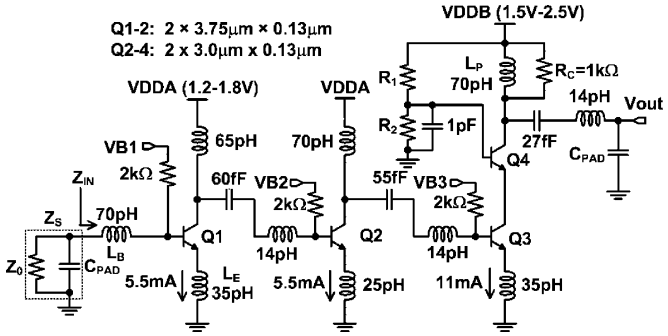

Fig. 3. 1.8-V/2.5-V three-stage 77-GHz LNA schematic.

across the array. Due to the severity of the power consumption problem, subsequent sections of this paper focus on the design of individual circuit blocks for low-power low-noise operation.

III. Circuit Analysis and Design

A. LNA

The schematic of the LNA is shown in Fig. 3. The first two stages are common emitter, which minimizes the NF. All stages are simultaneously noise and impedance matched using the techniques described in [34] and [35]. With the choice of the ratio of R_1 and R_2 in accordance with (1) as follows, where $V_{\mathrm{DDB\text{-}MIN}}$ is the minimum required value of V_{DDB}, the LNA is capable of sub-1.5 V operation.

$$\frac{R_1}{R_2} \leq \frac{V_{\mathrm{DDB-MIN}}}{V_{\mathrm{BE-ON}} + V_{\mathrm{CE-SAT}}} - 1 \tag{1}$$

To minimize the LNA NF, the HBTs must be biased at minimum NF current density. Next, the emitter length of Q_1 is chosen such that the real part of its optimum noise impedance is 50 Ω [34]. However, in the W-band, the pad capacitance (C_{PAD}), appears in parallel with the source impedance and cannot be neglected in the noise and impedance-matching methodology [34]. The effective source impedance (Z_S in Fig. 3) is now given by (2), where C_{PAD} is the pad capacitance, Z_0 is normally 50 Ω, and k is given by (3). Since the real part of Z_S is now a factor of k smaller than 50 Ω, the emitter length must be a factor of k larger than if the pad capacitance were not present. C_{PAD} was extracted using Calibre and found to be 32 fF, which yields $k = 1.6$ at 77 GHz.

$$Z_S = \frac{Z_0}{k} - j\frac{\omega C_{\mathrm{PAD}} Z_0^2}{k} \tag{2}$$

$$k = 1 + \omega^2 C_{\mathrm{PAD}}^2 Z_0^2 \tag{3}$$

The input impedance (Z_{IN} in Fig. 3) of the emitter degenerated amplifier, which is given by (4), must now be conjugately matched to Z_S. In (4), g_m includes the effect of the intrinsic emitter resistance, and ω_T is the cutoff frequency of Q_1 biased at minimum NF current density. The required values for components L_E and L_B are given by (5) and (6), respectively.

$$Z_{\mathrm{IN}} = R_{B1} + R_{E1} + \omega_T L_E + j\left(\omega L_E + \omega L_B - \frac{\omega_T}{\omega g_{m1}}\right) \tag{4}$$

$$L_E = \frac{1}{\omega_T}\left(\frac{Z_0}{k} - R_{B1} - R_{E1}\right) \tag{5}$$

$$L_B = \frac{Z_0^2 C_{\mathrm{PAD}}}{k} - L_E + \frac{\omega_T}{\omega^2 g_{m1}} \tag{6}$$

When the LNA stage is matched at the input and output, its gain is given by (7), where R_P is the total equivalent output resistance of the inductively loaded LNA stage at resonance, which includes the effect of R_C, the finite Q of L_P, and the cascode output resistance. A resistive load (R_C) is added on the final LNA stage to increase its bandwidth, which is otherwise low due to the high output resistance of the HBT cascode.

$$G = \frac{1}{4}\left(\frac{\omega_T}{\omega}\right)^2 \frac{R_P}{Z_0} \tag{7}$$

B. PA

Fig. 4 illustrates the PA schematic. The latter stages are common emitter to minimize power consumption and maximize power-added efficiency (PAE); the HBT sizes are scaled by a factor of 2 from stage to stage. The optimum scaling factor can be found using the methodology outlined in [36]. The optimal bias current density for the HBTs in the first stage of the PA is peak f_T/f_{MAX} current density because the first stage behaves like a linear amplifier. The latter stages, however, operate as class-B amplifiers. Using the measurement results illustrated in Fig. 5 [37], the bias current density of Q_3 and Q_4 is chosen to maximize the performance of the PA. The measurements show that the $\mathrm{OP}_{1\ \mathrm{dB}}$, P_{SAT}, and PAE all peak at the same current density.

C. Mixer, Balun, and IF Amplifier

The low-voltage millimeter-wave Gilbert cell mixer [8] and its connection to the LNA are illustrated in Fig. 6. To allow reduction of the supply voltage to 2.5 V, the RF pair is replaced by

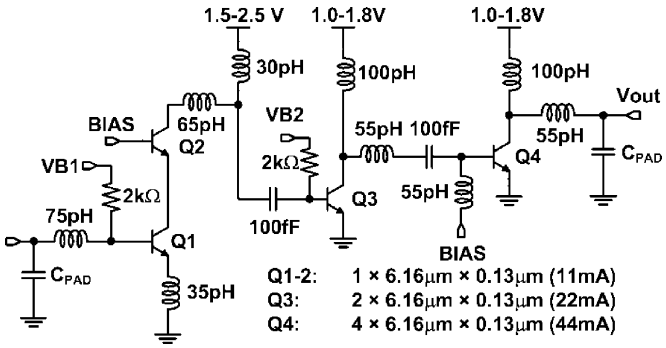

Fig. 4. 1.8-V/2.5-V 77-GHz three-stage PA schematic.

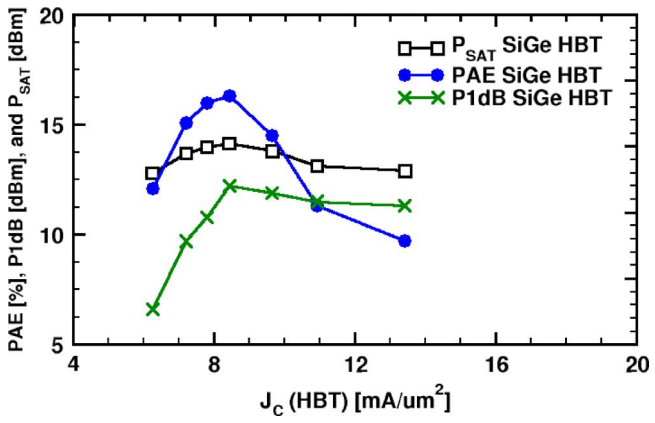

Fig. 5. Measured P_{SAT}, $\mathrm{OP}_{1\ \mathrm{dB}}$, and PAE versus bias current density in the final stage of the PA [37].

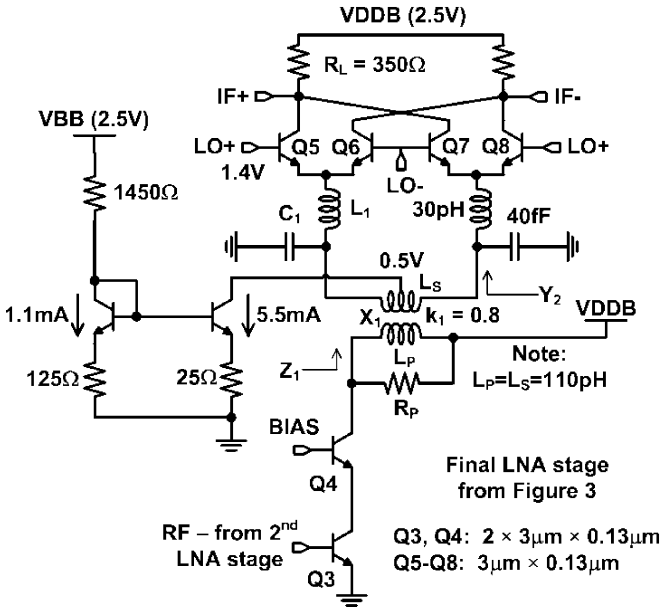

Fig. 6. Low-voltage double-balanced mixer without RF pair.

the secondary coil (L_S) of the transformer X_1, and the primary coil (L_P) becomes the load inductor of the final LNA stage. A current source biases the mixing quad through the center tap of the secondary winding. Components C_1 and L_1 are implemented using a 40-fF metal–insulator–metal (MIM) capacitor and 30 pH of interconnect, respectively.

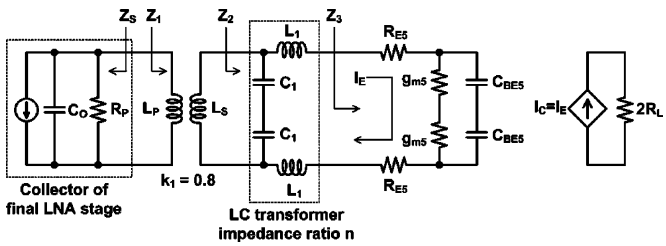

Fig. 7. Schematic of mixer used to calculate input impedance and gain.

To impedance match the mixer input to the LNA output, the schematic in Fig. 7 is used, where Z_3 is the differential input impedance looking into the emitters of Q_5–Q_8. The real and imaginary parts of the differential input impedance of the mixer (Z_3) are given by (8) and (9), where Q_5–Q_8 are assumed to be identical in size. With the correct choice of L_1 and C_1, the impedance at the input of the *LC* transformer (Z_2) is then given by (10). By adding the impedance transformation ratio n and tuning out the imaginary part of Z_3, L_1 and C_1 give the designer freedom to choose other component values.

$$\mathrm{Re}\{Z_3\} = 2R_{E5} + 2\frac{g_{m5}}{g_{m5}^2 + \omega^2 C_{\mathrm{BE5}}^2} \tag{8}$$

$$\mathrm{Im}\{Z_3\} = \frac{-2\omega C_{\mathrm{BE5}}}{g_{m5}^2 + \omega^2 C_{\mathrm{BE5}}^2} \tag{9}$$

$$Z_2 = n\,\mathrm{Re}\,(Z_3) \tag{10}$$

In general, the impedance looking into the primary coil of a transformer whose secondary coil is terminated in the real impedance R_T is given by (11), were L_P is the inductance of the primary coil, L_S is the inductance of the secondary coil, and k_1 is the coupling coefficient between the coils [38]. In this case, $R_T = Z_2$. The impedance Z_2 must be conjugately matched to the output impedance of the LNA cascode (Z_S), which is given by (12).

$$Z_1 = \frac{\omega^2 k_1^2 L_S L_P R_T + j\omega L_P\left(R_T^2 + \omega^2 L_S^2\left(1-k_1^2\right)\right)}{R_T^2 + \omega^2 L_S^2} \tag{11}$$

$$Z_S = \frac{R_P - j\omega C_0 R_P^2}{1 + \omega^2 C_0^2 R_P^2} \tag{12}$$

Using the parameter values listed in Table I, the numerical impedances Z_2, Z_1, and Z_S are given by (13)–(15). The choice of L_1 and C_1 has indeed reduced the imaginary part of Z_2 to zero, and the reflection coefficient (S_{11}) between Z_S and Z_1 is -15 dB, indicating reasonable matching.

$$Z_2 = 48\,\Omega - j2.7\,\Omega \approx 48\,\Omega \tag{13}$$

$$Z_1 = 18\,\Omega + j35\,\Omega \tag{14}$$

$$Z_S = 17\,\Omega - j76\,\Omega \tag{15}$$

D. VCO

A complete description of the differentially tuned accumulation-MOS (AMOS) varactor VCO and its design methodology is provided in [7].

TABLE I
CIRCUIT COMPONENT VALUES USED TO DEMONSTRATE MATCHING BETWEEN THE LNA AND MIXER

Parameter	Value
R_P	350Ω
C_0	25fF
ω	$2\pi 80\times 10^9$
R_{E5}	6.7Ω
g_{m5}	100mS
C_{BE5}	55fF
L_1, C_1	30pH, 40fF
L_P, L_S	110pH, 110pH
k_1	0.8

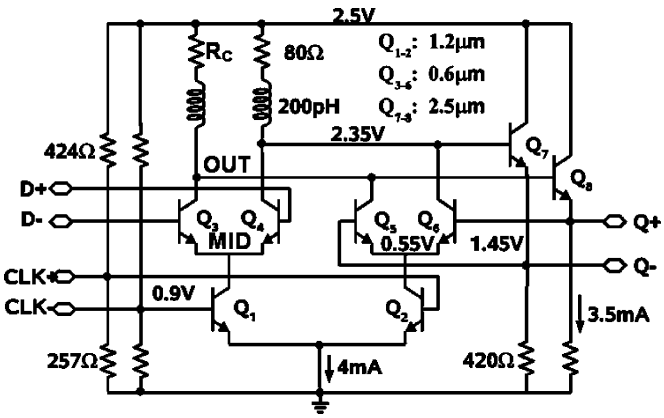

Fig. 8. Low-voltage D-latch with emitter followers.

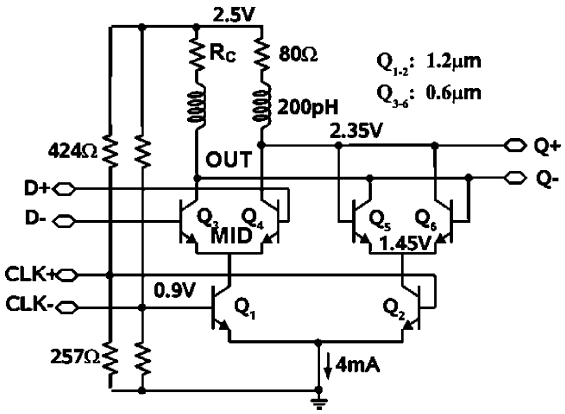

Fig. 9. Low-voltage D-latch without emitter followers.

E. Frequency Dividers

A static frequency divider contains two emitter coupled logic (ECL) latches (master and slave) in feedback. The typical topology for the ECL latch requires three HBTs and a resistor stacked between the supplies and, therefore, needs at least a 3.3-V supply [10].

In Figs. 8 and 9, two 2.5-V SiGe HBT latch topologies suitable for frequency division at 80 GHz are shown. To determine the superior latch design, two frequency dividers were designed and fabricated using the latches. In frequency divider A, the master and slave latches both have the architecture in Fig. 8, and in frequency divider B, the latches have the topology in Fig. 9.

To achieve 2.5-V operation, all current sources are replaced with biasing resistors, which also minimizes capacitance. The transistor sizes and bias currents for both latches are identical. HBTs Q_1–Q_6 are biased at peak f_T current density (when the clock and data inputs are balanced) and Q_7 and Q_8 are biased at 3/4 peak f_T current density. The latch load resistor (R_C in Figs. 8 and 9) and total current are chosen to provide 300-mV output swing, which ensures complete switching of an HBT differential pair over temperature variations. The peaking inductance is selected in accordance with (16) as follows, which extends the bandwidth by 85%.

$$L = \frac{C_L R_L^2}{1.41} \tag{16}$$

The maximum frequency at which a static divider will operate ($f_{D\mathrm{MAX}}$) depends on the applied input power. For small clock amplitudes, $f_{D\mathrm{MAX}}$ can be approximated using (17), where τ_{MID} is the time constant at the node marked MID in Figs. 8 and 9, and τ_D is the time constant at the node marked OUT. In (17), τ_{MID} represents the time required for Q_1 and Q_2 to switch the tail current from the latching pair (Q_5 and Q_6) to the D input pair (Q_3 and Q_4), and τ_D represents the time required for the input pair to transfer the data from the D input to the Q output. The entire process must occur within one-half of the clock period before Q_1 is switched off again.

$$f_{D\mathrm{MAX}} \approx \frac{1}{2\left[\tau_{\mathrm{MID}} + \tau_D\right]} \tag{17}$$

Frequency dividers are not robust to temperature variations when operating close to $f_{D\mathrm{MAX}}$. Moreover, (17) is an approximation for small clock amplitudes, and calculating τ_D while Q_1 and Q_2 are switching is not straightforward. However, the input-equivalent self-oscillation frequency (f_{OSC}) of the divider has been shown to track $f_{D\mathrm{MAX}}$ [10], and is given by (18), where τ_{D1} is the delay from the D input to the Q output of the master latch, τ_{D2} is the analogous delay for the slave latch. Normally, τ_{D1} and τ_{D2} are equal, but τ_{D2} is larger if the slave latch is loaded by additional circuitry such as another divider stage. The two delays can be derived using the open-circuit time constants method, and should be designed to provide the maximum sensitivity at the frequency of interest at the maximum operating temperature. Finding τ_{D1} and τ_{D2} for the calculation of f_{OSC} is simple because Q_1 and Q_2 are not switching.

$$f_{\mathrm{OSC}} = \frac{1}{2\left(\tau_{D1} + \tau_{D2}\right)} \tag{18}$$

In a frequency divider designed with two latches having the topology in Fig. 8, emitter followers Q_7 and Q_8 appear within the feedback loop formed by the master and slave latches. If Q_7 and Q_8 are too small, they cannot drive the latch clock inputs Q_1 and Q_2. However, if Q_7 and Q_8 are too large, they cannot be driven by Q_3–Q_6. Therefore, they have an optimum size, which is best determined through simulation, but can also be analyzed using time constants. Shown in Fig. 10 is the simulated f_{OSC} and power consumption of the latch in Fig. 8 versus the emitter length of Q_7 and Q_8 biased at a constant current density of 3/4 peak f_T/f_{MAX} current density. Also shown is the self-oscillation frequency calculated under the same conditions using (18).

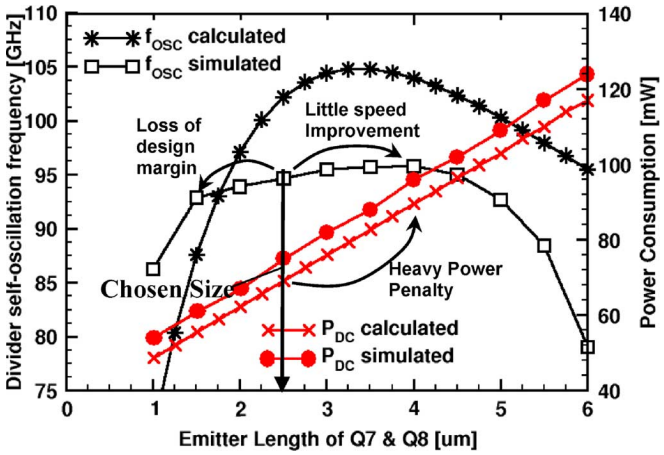

Fig. 10. Simulated and calculated self-oscillation frequency of frequency divider A versus the size of Q_7 and Q_8.

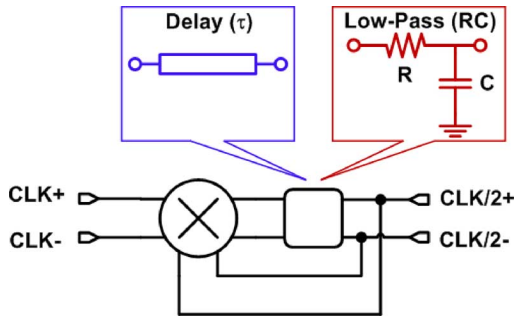

Fig. 11. Block diagram of a Miller divider.

Although the theoretical $f_{\rm OSC}$ is optimistic, the theory predicts the simulated behavior, including the optimum emitter length for Q_7 and Q_8.

An alternative topology for a broadband 2.5-V millimeter-wave frequency divider is the Miller divider, which, as shown in Fig. 11, consists of a mixer and a delay or filter element in feedback. The theory of operation of the Miller divider is available in [14]–[16], and its frequency range of division depends primarily on the cutoff frequency of the low-pass filter. The upper and lower frequency limits are given by (19) as follows:

$$\frac{2}{3}\frac{1}{2\pi RC} \le f_0 \le 2\frac{1}{2\pi RC} \tag{19}$$

The implementation of the Miller divider is illustrated in Fig. 12. Contrary to the ideal representation of the Miller divider, poles at the collectors of Q_3–Q_6 and at the emitters of Q_7 and Q_8 both influence the frequency range because neither is dominant. Shunt-series inductive peaking is used to maximize the bandwidth at the transconductor input (the bases of Q_1 and Q_2). The interconnect inductance between the outputs of Q_7 and Q_8 and the transconductor pair input (bases of Q_1 and Q_2) must also be accurately modeled. Optimization of the size of the Miller divider emitter followers relative to the mixing quad is accomplished in a similar fashion as presented for the static frequency divider.

The static divider with emitter followers, the static divider without emitter followers, and the Miller divider were each separately fabricated on individual test chips. In each case, the chip

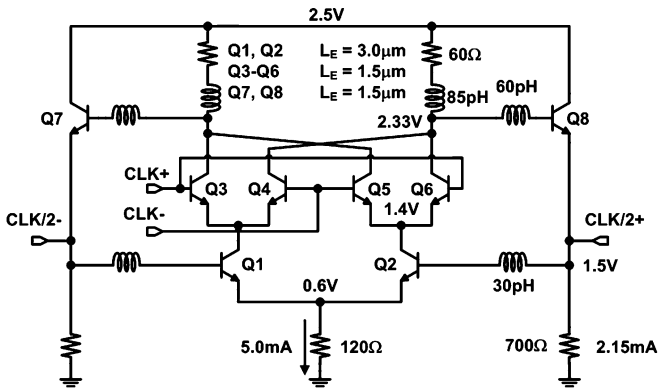

Fig. 12. Schematic of the implemented Miller divider.

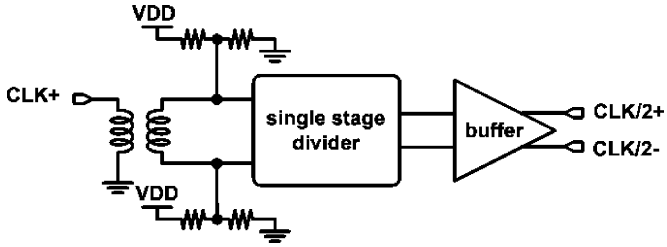

Fig. 13. Block diagram of the frequency divider test chip.

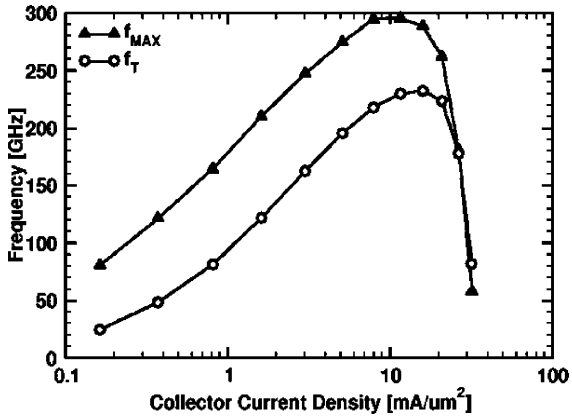

Fig. 14. Measured $f_T/f_{\rm MAX}$ versus collector current density at 1.2 V $V_{\rm CE}$.

architecture, illustrated in Fig. 13, is identical to ensure that the measurement results can be compared directly.

IV. Layout and Fabrication

All individual circuit blocks were fabricated in a 230-GHz f_T 300-GHz $f_{\rm MAX}$ 130-nm SiGe HBT process (no MOSFETs), and measurements were performed on-wafer with microwave probes. The f_T and $f_{\rm MAX}$ current density of the HBTs are shown versus collector current density in Fig. 14, which confirms the peak $f_T/f_{\rm MAX}$ to be 14 mA/μm^2. The SiGe HBT process has a six-metal copper back end of line (BEOL), and the design and layout of passive devices is discussed in [39] and [40].

The receiver was manufactured in an SiGe BiCMOS process with $f_T/f_{\rm MAX}$ of 220/250 GHz. The 130-nm MOSFETs are only used to implement accumulation mode varactors in the VCO, which provide superior phase noise and tuning range over

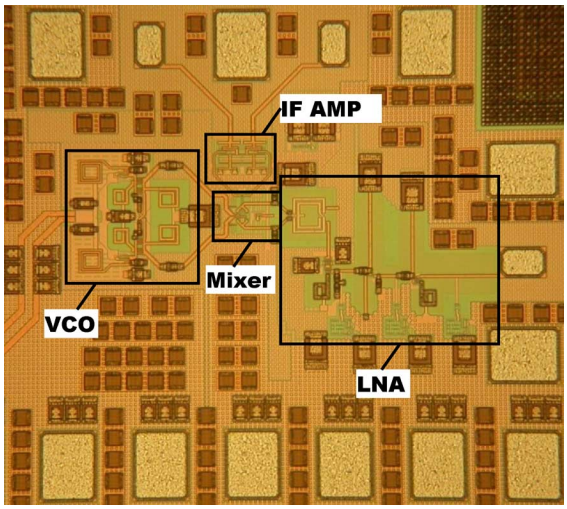

Fig. 15. Die photograph of the receiver (LNA, VCO, mixer, and IF amplifier). (515 μm$\times$ 460 μm).

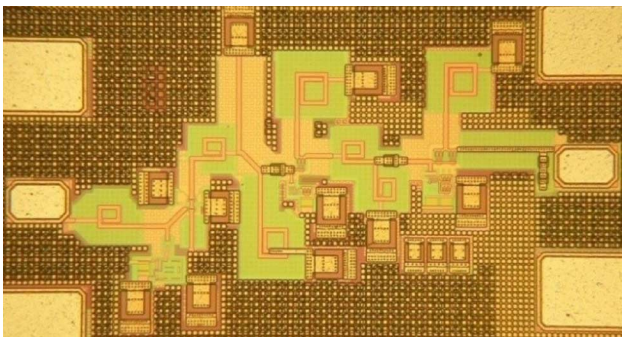

Fig. 16. 77-GHz PA layout with pads (390 μm$\times$ 280 μm).

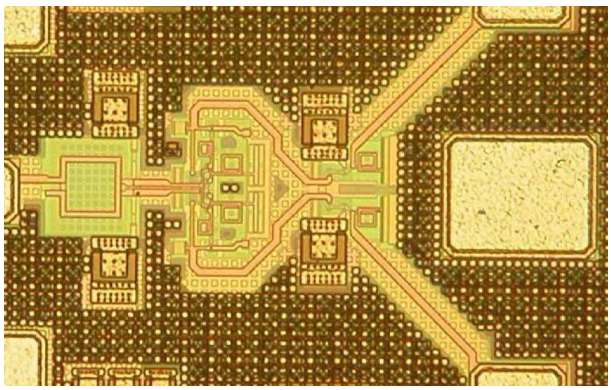

Fig. 17. Miller divider die photograph (250 μm$\times$ 180 μm).

HBT varactors [7]. Also provided in the SiGe BiCMOS process is a thick-metal BEOL.

A die photograph of the receiver, including the LNA, VCO, and mixer with on-chip balun and IF amplifier, is shown in Fig. 15. A die photograph of the 77-GHz PA is shown in Fig. 16, and a die photograph of the Miller divider is illustrated in Fig. 17. The die areas are indicated in the figure captions, and are small in comparison to other circuits reported in the literature because lumped inductors are used in place of transmission lines.

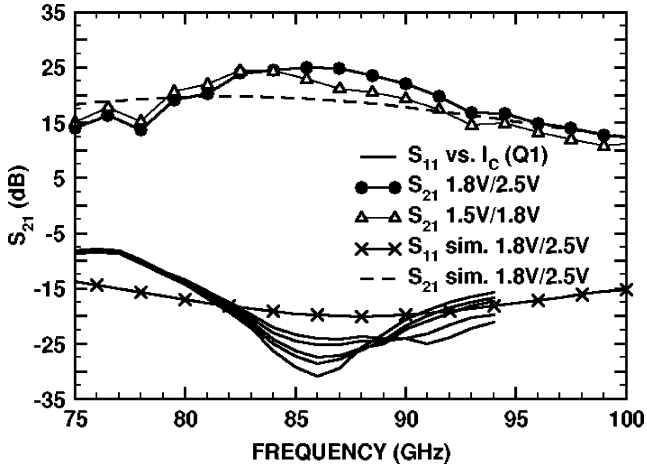

Fig. 18. Simulated and measured LNA S-parameters at 1.8-V/2.5-V and 1.5-V/1.8-V supply.

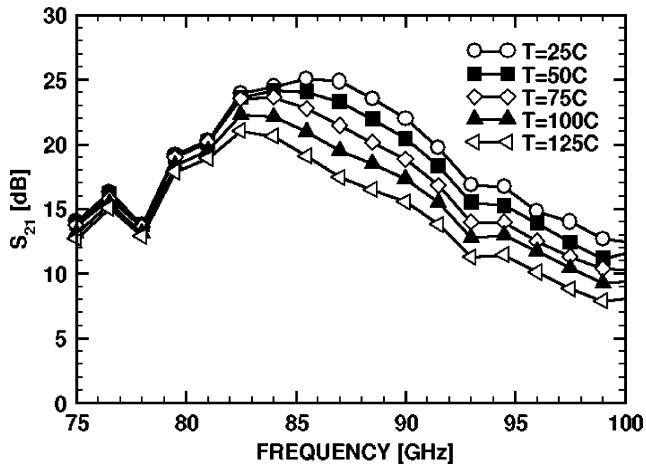

Fig. 19. Measured LNA S-parameters over temperature.

V. Simulation and Measurement Results

A. LNA

The LNA power gain (S_{21}) is shown in Fig. 18, measured at 1.8-V/2.5-V and 1.5-V/1.8-V supplies. The LNA achieves 25-dB peak power gain at 86 GHz with a $-$3-dB bandwidth of 7 GHz, and is operable down to 1.5-V/1.8-V supply with only 2-dB gain reduction. The input return loss, less than $-$15 dB from 80 to 94 GHz, is shown on the same plot for different bias current densities of the input transistor Q_1. The LNA gain was also measured over temperature, as illustrated in Fig. 19, and maintains 20-dB gain even at 125 °C.

B. PA

The PA S-parameters were measured from 57 to 94 GHz over temperature and are illustrated in Fig. 20. The input return loss is less than $-$15 dB from 70 to 90 GHz. In Fig. 21, measurements at 77 GHz show the PA achieves small-signal S_{21} of

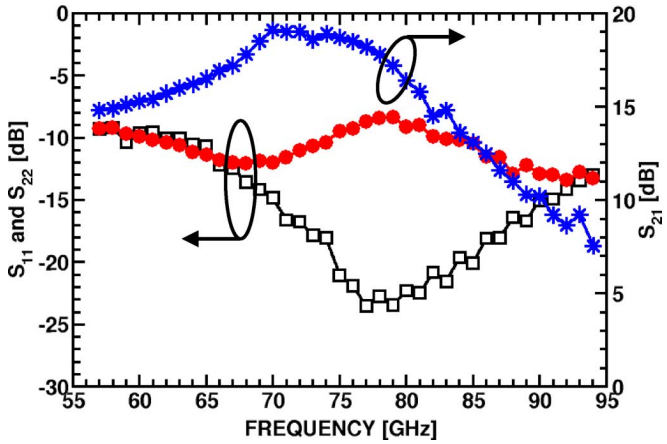

Fig. 20. PA S-parameters (saturated S_{21}).

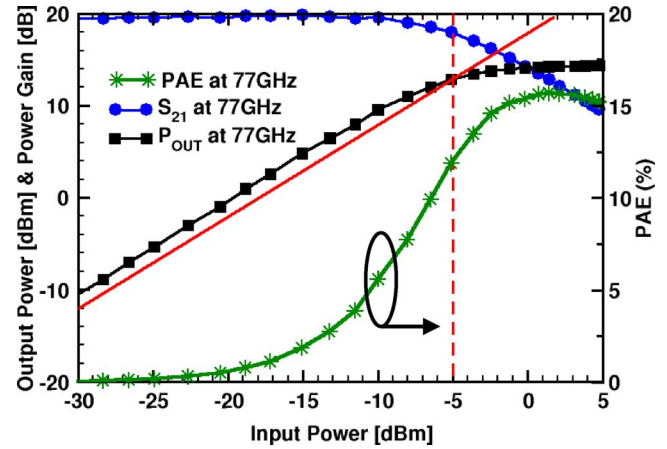

Fig. 21. Measured PA S_{21}, $\mathrm{OP}_{1\ \mathrm{dB}}$, and P_{SAT} at 77 GHz.

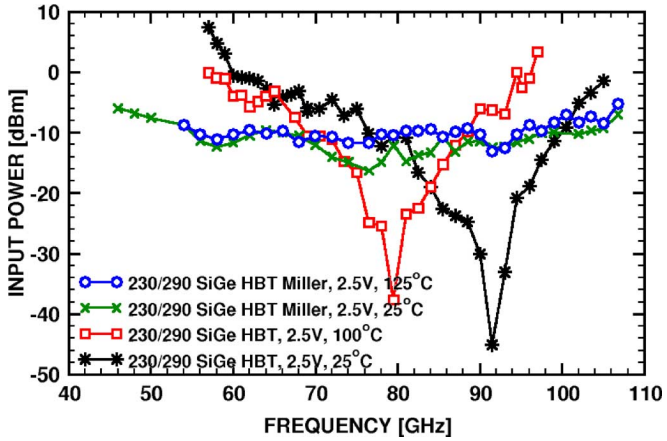

Fig. 22. Measured input sensitivity of frequency divider A and the Miller divider versus temperature.

19 dB, saturated output power of +14.5 dBm, an $\mathrm{OP}_{1\ \mathrm{dB}}$ of 12 dBm, and PAE of 15.7% (based on 161-mW P_{DC}). To the authors' knowledge, 15.7% PAE represents a record for silicon PAs above 60 GHz.

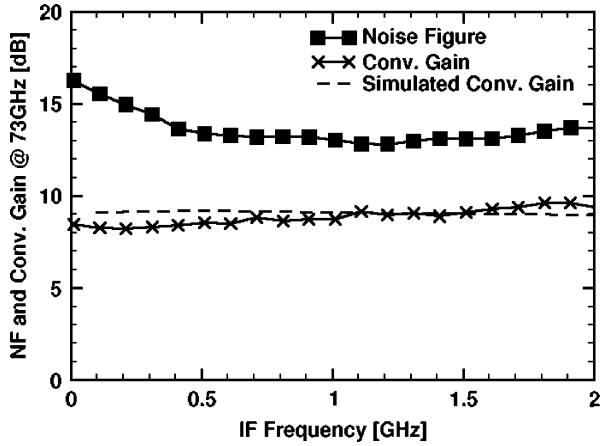

Fig. 23. Measured and simulated Mixer + IF amplifier NF and conversion gain at 73-GHz LO.

TABLE II
SiGe BiCMOS Receiver Power Consumption

Circuit Block	P_{DC} (mW)	
LNA	1.5V/1.8V	37mW
Mixer	1.5V	10mW
IF amplifier	1.5V	30mW
VCO	1.8V	46mW
TOTAL		123mW

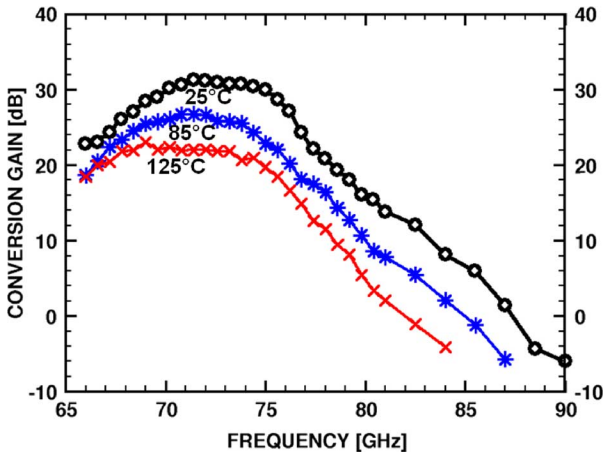

Fig. 24. Measured conversion gain of the SiGe BiCMOS receiver versus RF frequency and temperature at 76-GHz LO.

C. Frequency Dividers

Static frequency divider A, where both master and slave latches have emitter followers at their outputs, achieves an input-equivalent self-oscillation frequency of 91 GHz at 25 °C and 67 GHz at 125 °C, the highest ever reported for a silicon static frequency divider, while consuming only 75 mW from a 2.5-V supply. The previous silicon record was 76 GHz at 25 °C and 122 mW from 3.3 V [10]. The self-oscillation frequency was measured on several wafers, and was found to be in the 86–91-GHz range. The measured f_{DMAX} for this static divider was 105 GHz. Static frequency divider B, containing the latch

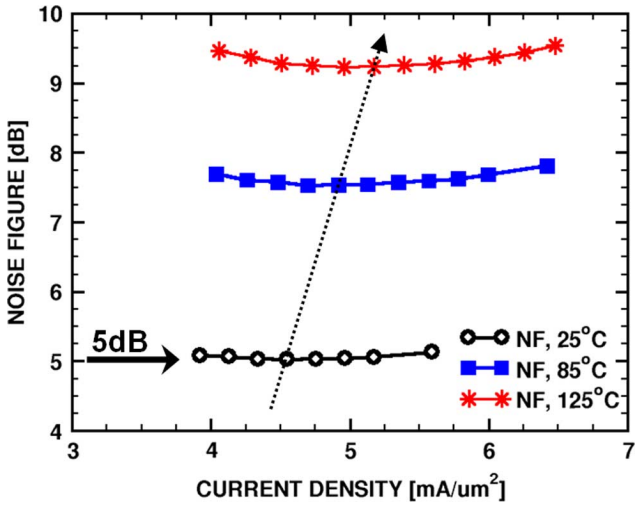

Fig. 25. Measured receiver DSB NF versus current density in the LNA and temperature for 75-GHz LO and 77-GHz RF.

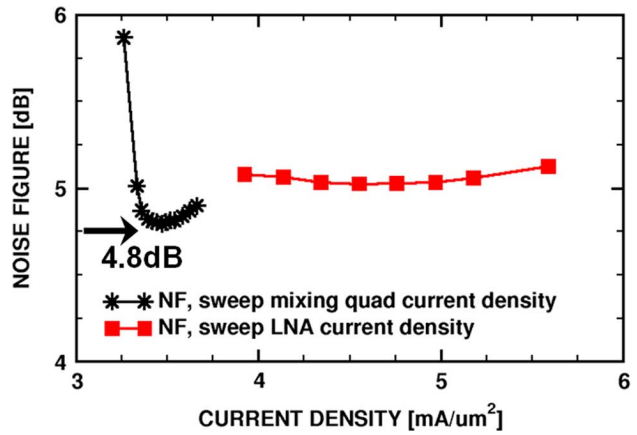

Fig. 26. Measured receiver DSB NF versus current density in the LNA and current density in the mixer for 75-GHz LO and 77-GHz RF.

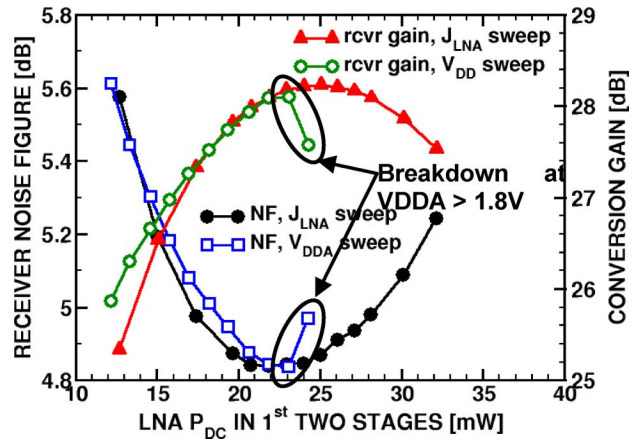

Fig. 27. Measured receiver NF and conversion gain versus LNA power consumption.

without emitter followers, has a self-oscillation frequency of only 70 GHz at 25 °C.

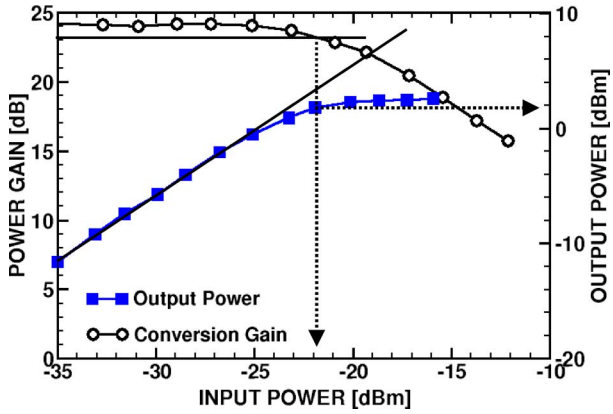

Fig. 28. Measured receiver gain compression at 77 GHz.

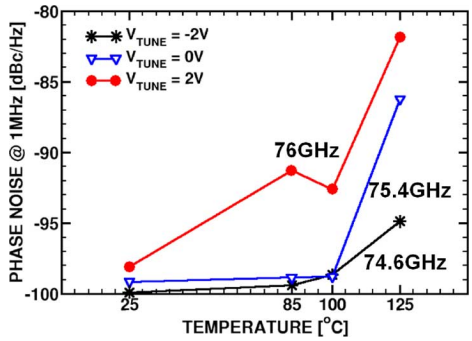

Fig. 29. Receiver phase noise measured at IF versus temperature and tuning voltage.

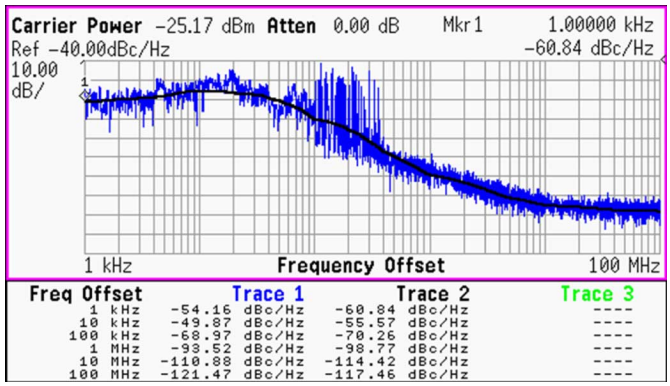

Fig. 30. Phase noise measurement at 100 °C, and $V_{\mathrm{TUNE}} = 0$ V.

The Miller divider consumes 33 mW and divides from 45 GHz up to 107 GHz at 25 °C. At 125 °C, the upper end of the frequency range remains 107 GHz. The measured sensitivity curves for all three dividers are shown in Fig. 22, with waveguide transition, cable, decoupling capacitor, and probe losses deembedded. Contrary to previous efforts [10]–[17], these measurements confirm that temperature robust W-band dividers with sub-100-mW power dissipation and 2.5-V supply can be designed for 77-GHz and 100-Gb/s applications.

Surprisingly, the division range of the static divider is less than that of the Miller divider. The 3.3-V static divider with tail current source in [10] operates down below 20 GHz, limited by

TABLE III
COMPARISON OF STATE-OF-THE-ART 77-GHz SiGe HBT FREQUENCY DIVIDERS ($\mathbf{FOM = f_{MAX}/P_{DC}}$)

Technology	P_{DC} (mW) & V_{DD} (V)	f_{OSC} (GHz)	f_{MAX} (GHz)	Topology	FOM (25°C)
65nm GP CMOS [17]	20, 1.2V	80	91	Static FF	4550
230/300 f_T/f_{MAX} SiGe HBT	**33, 2.5V**	**N/A**	**107**	**Miller**	**3242**
90nm SOI CMOS [11]	52, 2.2V	92	100	Static FF	1923
230/300 f_T/f_{MAX} SiGe HBT	**75, 2.5V**	**91**	**105**	**Static FF**	**1400**
405/370GHz f_T/f_{MAX} InP/InGaAs DHBT [13]	90, 3.8V	95	144	Static FF	1600
230/300 f_T/f_{MAX} SiGe HBT [10]N	122, 3.3V	77	100	Static FF	820
200GHz f_T SiGe HBT [14]	225, 4.5V	N/A	110	Miller	489
225GHz f_T SiGe HBT [12]	340, 5.2V	65	110	Static FF	324
245/370 f_T/f_{MAX} InP/InGaAs DHBT [15]	357, 5.5V	N/A	150	Miller	420
225 f_T SiGe HBT [16]	650, 5.5V	N/A	160	Miller ÷4	246

TABLE IV
COMPARISON OF STATE-OF-THE-ART 77-GHz SiGe HBT PAs ($\mathrm{FOM} = f^2 \times \mathbf{G} \times \mathbf{P}_{\mathrm{SAT}} \times \mathrm{PAE}$)

Technology	freq (GHz)	Gain (dB)	P_{SAT} (dBm)	PAE (%)	Area (mm^2)	Topology	FOM (25°C)
200/200 f_T/f_{MAX} SiGe HBT [2]	77	17	+17.5	12.8	1.35×0.45	4-stg CE	2139
200/290 f_T/f_{MAX} SiGe HBT [9]	77	6.1	+12.5	3.5	2.1×0.75	2-stg CE	15
230/300 f_T/f_{MAX} SiGe HBT	**77**	**19**	**+14.5**	**15.7**	**0.3×0.5**	**1-stg casc. + 2-stg CE**	**2083**

the transformer bandwidth, and it is suspected that the removal of the tail current source is responsible for the reduction in the frequency range.

D. Down-Conversion Mixer and IF Amplifier

The mixer and IF amplifier together achieve a differential to single-ended conversion gain of 8–11 dB, and an NF of 12.8–14.5 dB for a −2 dBm, 73-GHz LO signal, and 1 GHz IF, as shown in Fig. 23, alongside simulation results for the same LO amplitude and bias conditions. The mixer could not be measured at 77 GHz because only one signal source is available in the 75–110-GHz range. However, receiver measurements will confirm operation of the mixer above 73-GHz LO. The NF also includes the insertion loss of the transformer, larger than 2 dB, at the RF port of the mixer.

E. Receiver

The SiGe BiCMOS receiver (block diagram illustrated in Fig. 2) designed using the circuit blocks presented here was measured at 1.5-V/1.8-V supplies and has been found to be competitive with state-of-the-art SiGe HBT and CMOS results in terms of RF performance and power consumption. In Table II, the power consumption of each circuit block in the SiGe BiCMOS receiver is listed, for a total of only 123 mW. If the power dissipation of the IF amplifier is excluded, the receiver consumes only 93 mW.

In Fig. 24, the conversion gain and NF of the SiGe BiCMOS receiver with a constant 76-GHz on-chip LO is shown. The receiver achieves a maximum of 31-dB conversion gain at 73 GHz and a −3-dB bandwidth of 7 GHz. At 125 °C, the receiver maintains 22-dB peak conversion gain. The emitter width of the HBTs in the SiGe BiCMOS process is 190 nm in comparison to 130 nm in the HBT-only process. The resulting increases in C_{BE} and C_{BC} shift the center frequency of the receiver downward from the desired value of 77 GHz.

The NF of the SiGe BiCMOS receiver has been measured versus current density in the LNA (76-GHz LO, 1-GHz IF), and the results are illustrated in Fig. 25. The receiver achieves a double-sideband (DSB) NF of 5 dB at 25 °C and 9.2 dB at 125 °C for a 75-GHz LO and 77-GHz RF. The minimum receiver NF occurs when the current density in the LNA transistors is 4.5 $\mathrm{mA}/\mu\mathrm{m}^2$. The measurements indicate a weak upward trend of the optimum NF current density with increasing temperature. However, the dependence is negligible, and for simplicity, the LNA should be biased at constant current versus temperature for optimum noise performance.

The NF of the receiver was also measured versus the current density in the mixing quad of the down-conversion mixer. The results, illustrated in Fig. 26 using "$*$" symbols, shows that the optimum current density of the mixing quad is 3.4 $\mathrm{mA}/\mu\mathrm{m}^2$, as opposed to 4.5 $\mathrm{mA}/\mu\mathrm{m}^2$ in the LNA. Also note that the receiver NF has improved to 4.8 dB by optimization of the mixer bias. The lower optimum current density in the mixing quad may arise because the HBTs are easier to switch at lower current density. However, the HBTs in the LNA are in a common-emitter configuration, whereas the HBTs in the mixing quad are in a common-base configuration, which may also impact the optimum NF current density. As a final note, the input impedance of the common-base mixer, given by (11), is sensitive to the g_m of Q_5–Q_8, which, in turn, is sensitive to the mixer bias current. As a result, the receiver NF increases rapidly if the mixing quad bias departs from its optimum value. The noise-figure degradation is greater at low current and, therefore, the current density in the mixing quad should be guaranteed to fall at or above the optimum value over temperature variations.

To further reduce the power consumption of the SiGe BiCMOS receiver, the bias current density or power supply

TABLE V
COMPARISON OF STATE-OF-THE-ART 77-GHz SiGe HBT RECEIVERS

Technology	RF/LO (GHz)	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	P_{DC} (mW)	Area (mm^2)	Notes
170/200GHz f_T/f_{MAX} SiGe HBT [28]	77/77	26	9	-24	230	0.6×0.5	Single-chip transceiver. Area & P_{DC} for RX only.
250 f_{MAX} SiGe HBT [29]	77/52	35	8	-27.5	186	6.8×3.8 (×4 array)	×4 transceiver array P_{DC} for RX + VCO only.
330 f_{MAX} SiGe HBT [27]	77/77	30	11.5 (SSB)	-26	440	0.71×0.95	VCO, LNA, Mixer
250 f_{MAX} SiGe HBT [26]	77/77	40	Not Given	-38	195	1.7×1.1	VCO, LNA, Mixer, IF-amp
65nm GP CMOS [24]	85/85	12	9	-13	94	0.50×0.46	LNA, Mixer, IF-amp
65nm GP CMOS [30]	85/90	12.5	8	-18	206	1.1×0.6	LNA, Mixer, IF-amp, VCO, frequency divider
220/250 f_T/f_{MAX} SiGe BiCMOS	**76/77**	**24**	**4.8**	**-21.7**	**123**	**0.52×0.46**	**VCO, LNA, Mixer, IF-amp**

voltage of the LNA could be reduced. Naturally, doing so would increase the receiver NF and reduce the conversion gain. An important question can be asked of such an experiment: which incurs the smaller NF and/or conversion gain penalty: reducing the power supply of the LNA ($VDDA$ in Fig. 3) at constant current density, or reducing the bias current density in the LNA at constant supply voltage? Shown in Fig. 27 is the receiver conversion gain and NF measured versus the power consumption in the first two stages of the LNA. In solid symbols, the variation in power consumption is realized by changing the bias current density, and in open symbols by changing the power supply voltage. The results show that reducing the power supply voltage or bias current density are approximately equivalent in terms of their impact on receiver NF and conversion gain.

Illustrated in Fig. 28 are the measured gain compression characteristics of the SiGe BiCMOS receiver for a 76-GHz LO and 77-GHz RF. The receiver has an $OP_{1\,dB}$ of $+1.8$ dBm and an $IP_{1\,dB}$ of -21.6 dBm.

The stringent phase noise specifications of frequency-modulated continuous-wave (FM-CW) radar systems must be met at 125 °C, particularly in automotive applications. Although phase noise of less than -100 dBc/Hz @ 1-MHz offset has been previously demonstrated at 25 °C in W-band SiGe VCOs [7], to the authors' knowledge, the phase noise of W-band SiGe BiCMOS VCOs has not been reported over temperature.

The phase noise of the receiver with unlocked VCO was obtained by measuring the phase noise at IF. An RF signal, with phase noise far below that of the receiver, was applied at 77 GHz, yielding a down-converted LO spectrum centered at 1.5–3.0 GHz, depending on the VCO tuning voltage. The phase noise of this spectrum was measured at 25 °C, 85 °C, 100 °C, and 125 °C. The results, illustrated in Fig. 30, show that phase noise of -98.5 dBc/Hz at 1-MHz offset is obtainable up to 100 °C, and sub -95 dBc/Hz at 1-MHz offset is obtainable up to 125 °C. Fig. 29 confirms the data in Fig. 30 with a screenshot of the measurement at 75-GHz LO and 100 °C. The rapid degradation in phase noise at 125 °C is likely caused by a sudden loss in negative resistance.

VI. CONCLUSION

The first 2.5-V 77-GHz SiGe BiCMOS receiver with record 4.8-dB NF and 123-mW power consumption has been reported. Moreover, the receiver maintains -98.5-dBc/Hz phase noise up to 100 °C, and occupies only 450 μm× 280 μm of die area if pads are excluded. Also reported is record 15.7% PAE in W-band SiGe HBT PAs and low-power optimized designs for static and Miller frequency dividers. The performance of the receiver and chipset circuit blocks is compared to other published work in Tables II–V (this study represented via **bold text**). Circuit design techniques presented minimize power dissipation and NF while maintaining the margin needed to operate at 77 GHz and 100 °C. Measurements verify the performance of all circuit blocks over temperature and provide insight into the optimal bias current density for minimum noise in SiGe HBT mixers and LNAs, and maximum linearity and efficiency in SiGe HBT mixers and PAs.

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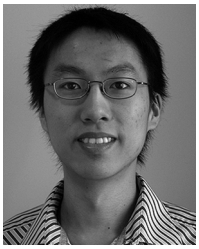

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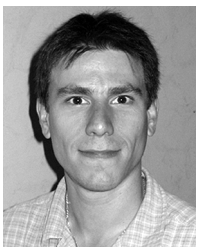

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