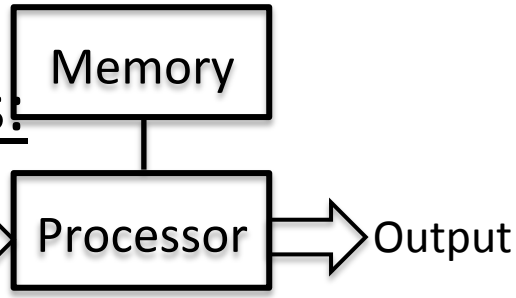
SISTEMI EMBEDDED
AA 2013/2014

SOPC Design Flow

Federico Baronti

An embedded system is a computer system that is **not** general-purpose like a personal computer

Main building blocks:



- Processor(s)
- Memories: FLASH, EEPROM, SRAM, SDRAM, DDRAM
- Peripherals: GPIO, Timer/Counter, PWM, Communication interfaces (SPI, I^2C, CAN,…), A/D, D/A,…
- …
- and definitely some “specific” SOFTWARE

An embedded system is a computer system that is **not** general-purpose like a personal computer

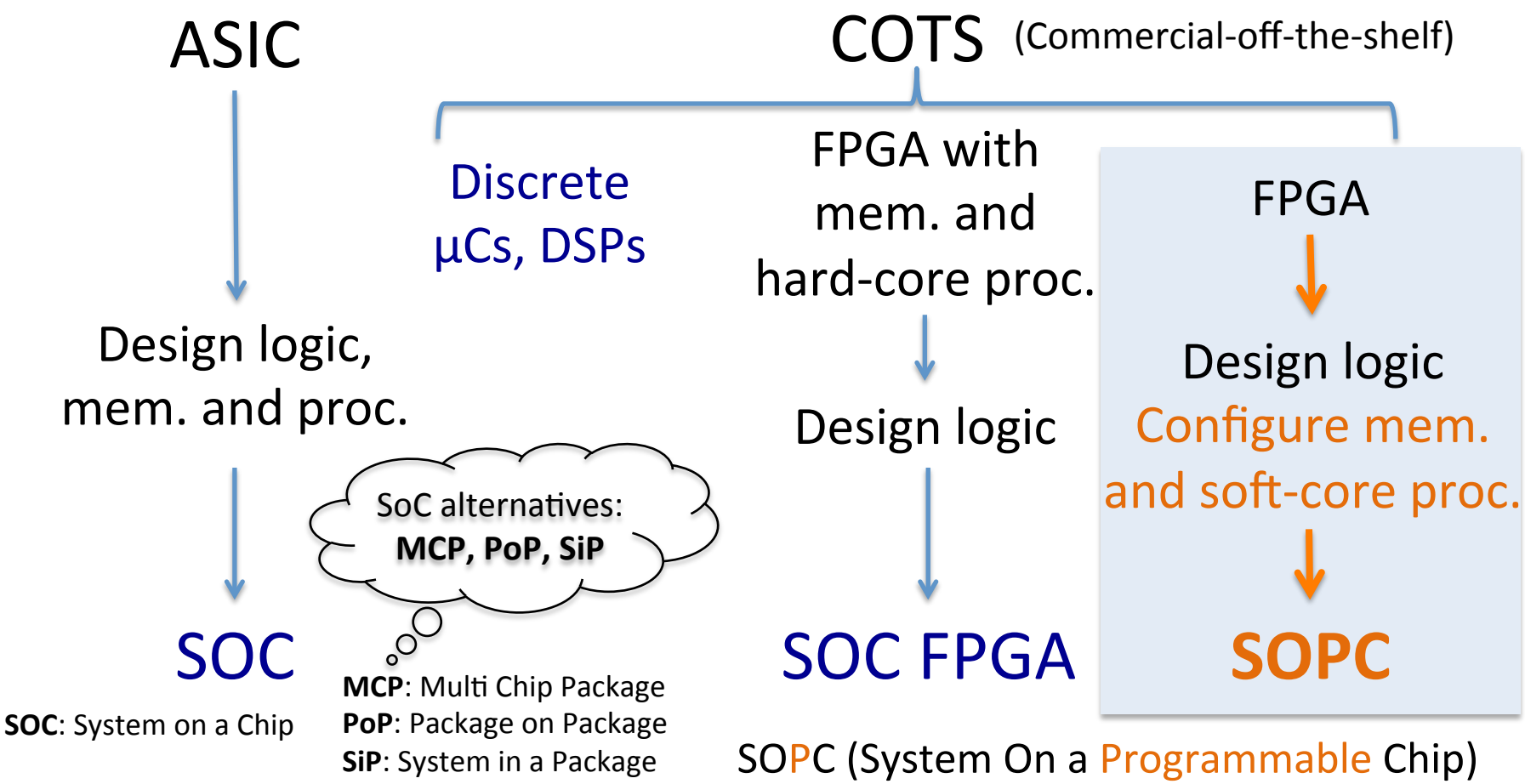
Main design constraints:

- Production cost
- Development cost (*Non-Recurring Engineering* cost)
- Power consumption
- Physical size

- Their relative importance varies from one embedded system to another

An embedded system is a computer system that is **not** general-purpose like a personal computer

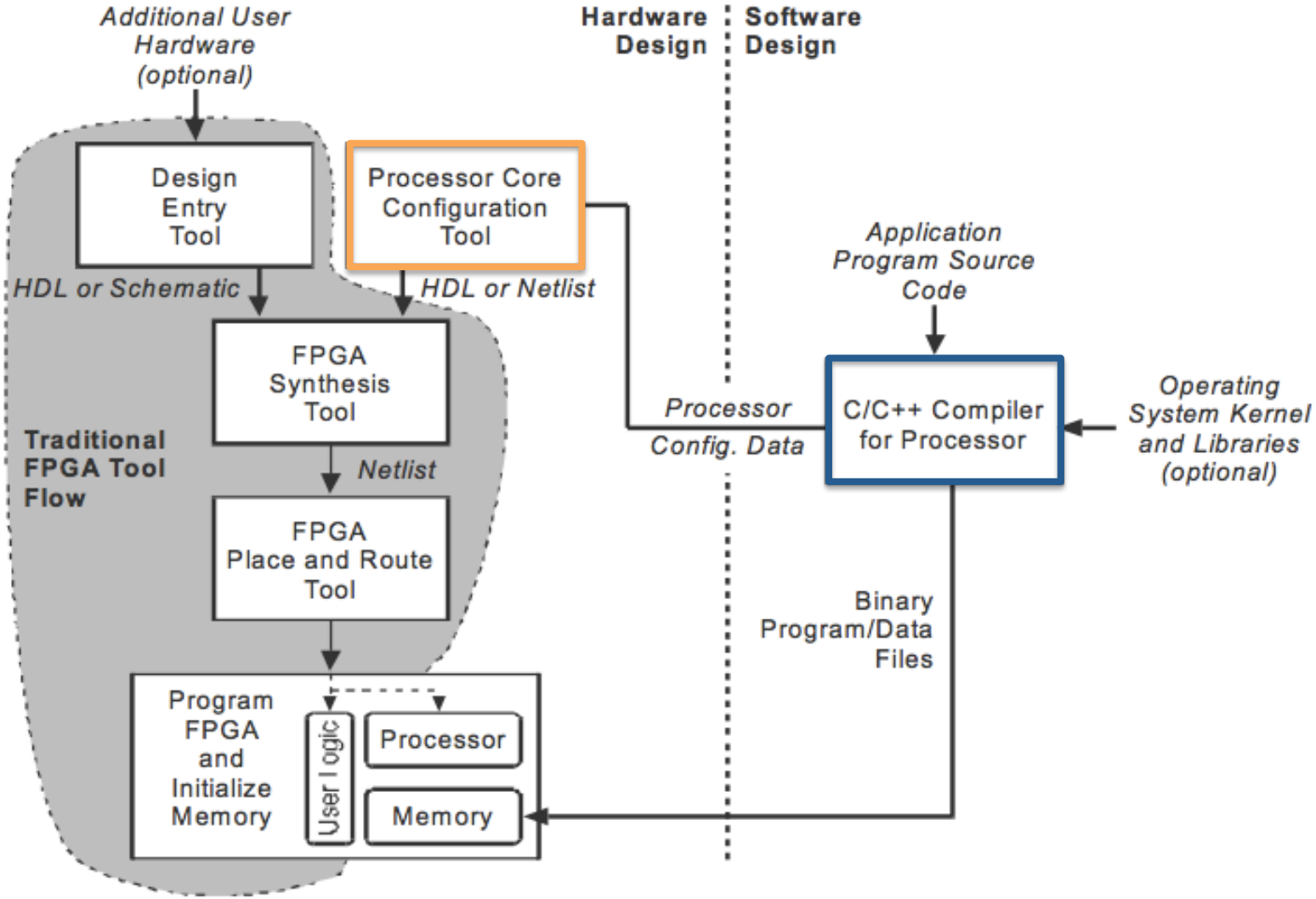
Hardware design options:



System-on-Programmable-Chip

- Configure soft-core processor:
  - Core configuration
    - Instruction/Data Cache, Pipeline Stages, JTAG Debug Modules, Custom Instructions, etc.
  - Peripheral configuration (what and where)
    - Peripheral selection
      - Standard peripherals from Altera and third-party vendors: GPIOs, Timers, Serial Communication Interfaces, Memory Interfaces, etc.
      - Custom peripherals
    - Address mapping

SOPC Design Flow



J. O. Hamblen et al. “Rapid Prototyping of Digital Systems – SOPC Edition”, Springer, 2008

Altera's **CAD** tools

- Logic Design: **Quartus II**
  - Nios II Configuration and SoPC integration: **Qsys (**SOPC Builder**)**
- Logic Simulation: **ModelSim-Altera**
- Software Development:
  Nios II Embedded Design Suite (EDS) – Eclipse

Embedded System course (1)

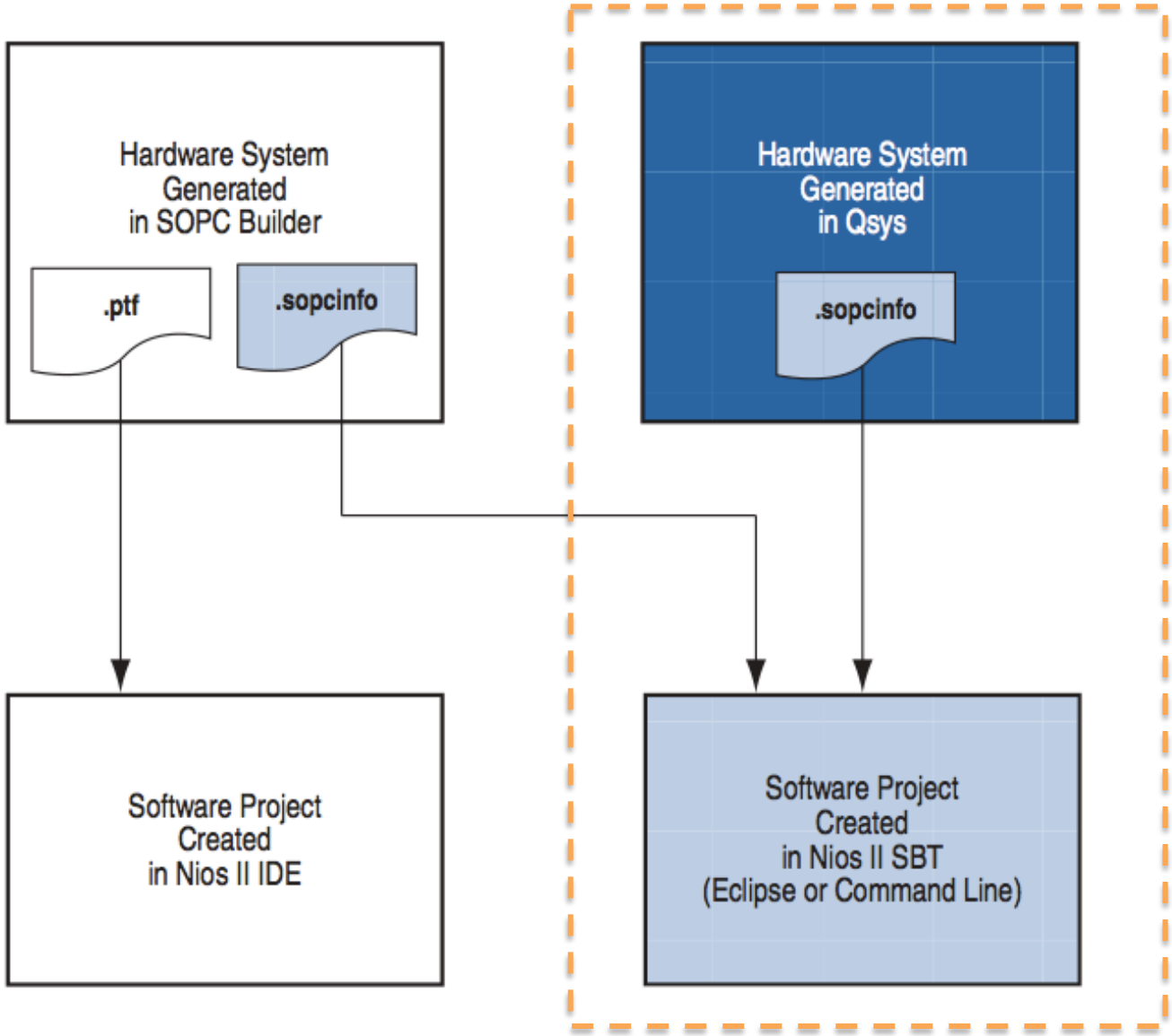
- Quartus II Web Edition Software (13.0sp1) http://dl.altera.com/13.0sp1/
  - Quartus II Software (includes Nios II EDS)
  - ModelSim-Altera Edition (includes Starter Edition)
  - Devices: Cyclone II, Cyclone III, Cyclone IV device support (includes all variations)
- University Program Installer (13.0)
  - http://www.altera.com/education/univ/software/monitor/unv-monitor.html
- Nios II Documentation
  - http://www.altera.com/literature/lit-nio2.jsp

Embedded System course (2)

- DE2: Development & Education board
  - Cyclone II EP2C35F672C6 (33216 LE; 105 M4K)

	Nios II/e	Nios II/s	Nios II/f
#LE	600-700	1200-1400	1400-1800
#M4K	2	2 + cache	3 + cache

Nios II HW/SW Design Flow



Nios II SBT Design Flow

- Creating a project
  - Nios II Application and BSP from Template
    - Target hardware information (.sopcinfo, CPU)
    - Project template
    - Board Support Package (BSP)
- Code editing (.c, .h)
- Building the Project (.elf)
- Configuring the FPGA
  - Quartus II programmer (.sof)
- Running/ Debugging the Project on Nios II
  - Run/Debug configurations

Board Support Package (BSP)

- Library and header files (e.g. system.h) specific to the target processor
- Automatically generated through .sopcinfo and CPU
- Hides memory map, available devices, device implementation and processor configuration
  - Device drivers
  - Hardware Abstraction Layer (HAL)
  - RTOS: Micrium MicroC/OS-II