Silicon Electrochemical Micromachining Technology: the Good, the Bad, and the Future

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Electrochemical micromachining (ECM) is a highly flexible technology allowing for accurate fabrication of both simple microstructures (e.g. macropores, microtips, spirals) and complex microsystems (e.g. microgrippers, microneedles) in silicon, at low cost in any lab. In this paper main advantages and drawbacks of ECM technology are discussed, also with respect to standard leading micromachining technology, and future directions for ECM advance are given.

Introduction

Silicon electrochemical micromachining (ECM) has come to a long journey since the pioneering paper of Lehmann and Foll, dated 1990 (1), which firstly reported about the possibility of controlling the anodic dissolution of silicon in HF-aqueous electrolytes by back-side illumination etching for the formation of nicely ordered array of macropores. Over the last 20 years understanding of anodic dissolution of silicon in HF-based aqueous electrolytes has greatly improved, especially for n-type silicon under back-side illumination (2-8), thus providing a fertile ground that allowed to elaborate the etching of novel microstructures (9-17), besides simple macropores. More recently, a further significant step forward has been moved by learning how to control in real time the anisotropy of electrochemical silicon dissolution (18), thus enabling the fabrication of complex microsystems through exploitation of functional and sacrificial structures (19-28). ECM has now acquired a degree of maturity that makes it a valid alternative to standard silicon etching technologies, at least at research level. Nowadays, ECM is routinely used to fabricate silicon microstructures (e.g. macropores, microtips, spirals) and microsystems (e.g. microgrippers, microneedles) with applications ranging from (bio)sensing (19, 20, 26, 27) to nanomedicine (21, 22), from photonics (23, 24) to microelectronics (25, 28).

Time-multiplexed etching process (TMEP) is today the leading technology for silicon microstructuring at industrial level. TMEP ensures high reliability and great flexibility in microfabrication, though a few major problems are still unsolved and act as a bottleneck towards novel applications, among which Through Silicon Vias for chip stacking. ECM exhibits quite unique features that allow overcoming (or smoothing) limitations of TMEP, thus making ECM an attractive alternative for silicon microstructuring at industrial level. For instance, aspect-ratio value of structures etched by ECM can be increased over 100 (18), verticality can be controlled to 90° with high accuracy (30), surface roughness can be reduced below 10 nm (31), etching anisotropy can be tuned in real time from 1 to 0 (and back) (18). Nonetheless, a number of significant constraints also exist for ECM and must be taken into account for silicon microstructuring at
industrial level. Among these, dependence of both minimum and maximum sizes of etched structures on silicon doping (5, 8), and significant reduction of etching rate as the depth of etched structures increases over 100 (5, 32) are worthy to be discussed. Finally, besides advantages and drawbacks above cited, the future of ECM (at industrial level) will probably depend on the scaling up of the technology to wafer level (diameter of about 200 mm) batch fabrication.

In this paper, main features and drawbacks of ECM technology are reviewed and discussed, also with reference to TMEP, and future directions for ECM advance at industrial level are also pointed out.

The Good and the Bad of ECM

ECM relies on the synchronized (both in time and space) electrochemical oxidation of silicon and subsequent silicon oxide removal in aqueous HF electrolytes under anodic biasing and back-side illumination of the silicon electrode (1, 4, 8). A major advantage of ECM over other microstructuring technologies is certainly connected with the possibility of fabricating complex silicon microstructures and microsystems in any lab by using a low cost setup. An ECM setup consists, in its basic configuration, of an HF-resistant electrochemical cell, a potentiostat-galvanostat, and a halogen lamp. The total cost would range from a few to ten thousands Euros, which is roughly one order of magnitude lower than that of etching technologies based on Reactive Ion Etching (RIE) reactors, among which TMEP in ICP-RIE reactor, also known as BOSCH method, is today the reference process for MEMS fabrication. Time-multiplexed deep silicon etching relies on alternating etching and passivation (polymerization) steps, e.g. using SF₆ as etch gas and CHF₃ and Ar as polymerization gases. Each polymerization step is followed by an etching step that fully removes the polymer layer at the bottom of etched features, while leaving unaltered the polymer layer on the sidewalls that are hence protected from etching. In spite of the high degree of flexibility, a few intrinsic constraints of TMEP, among which e.g. aspect ratio, scalloping, tilting, etching lag, and micrograss, limit somehow the achievement of new commercial outcomes. ECM technology allows overcoming some of the limitations of TMEP technologies, thus providing an alternative route to silicon microstructuring, though still at research level so far.

As to TMEP, aspect ratio (i.e. ratio between out-of-plane depth/height and in-plane size of microfabricated features) is commonly around 20-30 and has been pushed to a maximum value of 50 (33). A conventional TMEP produces peak-to-valley periodic scalloping (roughness) on the sidewall surface of etched structures, due to alternating etching and passivation steps, in the range of 100-200 nm, which reduces to 50 nm for well-controlled process (34). Optimization of both etch and passivation times further lessens sidewall scalloping to about 10 nm, though at expense of sidewall angle (etch profile) (35, 36). Etch profile depends on etching features (both size and depth) and, in turn, on aspect ratio. If the process is optimized to give a vertical profile (90°) for a certain critical feature size, larger features may result in negative profile angles (<90°) and smaller features may result in positive profile angles (>90°) (37). Etching rate as high as 20 µm/min have been reported for TMEP (38), although typical etching rate are around 2.5-3.5 µm/min. Moreover, etching rate significantly decreases as aspect ratio increases (≈10% variation for features with widths from 2.5-10 µm), a phenomenon known as
aspect ratio dependent etch –ARDE, and always tends to zero at some critical aspect ratio value depending on the set of process parameters (39). Etching rate also depends on pattern density, i.e. area of exposed silicon, for features with same size. This effect is known as loading and produces an etching rate that decreases as the density of exposed silicon increases (40). A further drawback of TMEP is known as micrograss, which is the term used to describe the formation of microcolumns of silicon owing to residual polymer left on the bottom surface after each etching step. Micrograss is influenced by feature size (both width and depth) and, in turn, aspect ratio, but it is likely to occur in features with larger than smaller sizes (37).

As to ECM, aspect ratio values exceeding 100 have been reported both for simple structures, e.g. ordered array of macropores, and complex microsystems (i.e. electrically-actuated microgrippers) (5, 18). In Ref. 18 thin silicon spring with length of 500 µm, width of 1 µm, and height over 100 µm have been fabricated to sustain and rotate the fingers of a microgripper totally fabricated by ECM technology. Surface roughness on sidewall of etched microstructures is typically around 50 nm for non-optimized ECM, but peak-to-valley roughness below 10 nm has been achieved by lowering the anodization voltage of the etching process (24, 31). Etch profile can be finely controlled by properly tuning the etching current over time independently of aspect ratio of etched structures, thus allowing to obtain either vertical or inclined profiles with controlled slope over depth. Vertical profiles with relative error of 1% over a depth of 100 µm have been reported for 2-mm-long trenches/walls with width of 2.8/1.2 µm (30). A peculiar advantage of ECM over TMEP is related to the possibility of changing the size of etched features as the etching progresses. This allows modulating the size of etched microstructures over depth, thus enabling the fabrication of sinusoidal-like and bubble-like shaped pores (3, 7, 15) and buried microchannels (41). Etching rate for standard ECM is commonly of a few µm/min, at least for etching depth up to 100 µm, regardless of size and aspect ratio of etched features, and no significant dependence on pattern density has been reported (5). As a matter of fact, microstructures with high uniformity, both in-plane and out-of-plane, have been reported, but ECM etching rate reduces according to the square root of time (5, 32). No micrograss has been reported for ECM, although other unwanted effects exist that limit etching outcomes, as it will be discussed in the following of this section.

Figure 1. SEM images, at different magnifications, of silicon trenches fabricated by ECM technology, highlighting the effect of both anisotropic and isotropic phases (After Ref. 18)
A further unique feature of ECM technology is the control of etching anisotropy in real time (as the etch progresses) from 1 (etching perfectly anisotropic) to 0 (etching perfectly isotropic), and back (within certain conditions) (18). An example of deep trenches etched in silicon using an initial anisotropic phase and a final isotropic phase is given in Figure 1. Anisotropy control enables the fabrication of complex 3D microsystems through the use of functional (to the microsystem fabrication) and sacrificial (sacrificed for the accurate microsystem fabrication) structures. Microelectromechanical systems (MEMS), optofluidic platforms, microneedle-based chips have been fabricated using a single-etching step with an initial anisotropic phase, which was used to etch the pattern deep in the substrate and create high-aspect-ratio microstructures, and a final isotropic phase, which was used to release part of the etched microstructures from the substrate and, eventually, yield them freestanding (19-27). A few amazing examples of microstructures and microsystems fabricated by ECM technology are given in Figures 2 and 3.

A coin has two sides. The other side of ECM is related to limitation of minimum/maximum size and spacing of etched features for CZ-grown n-type silicon substrates with standard doping of a few Ωcm, which are commonly employed for MEMS fabrication. Minimum size has been recently reported to be strictly dependent on spatial period for ordered macropore arrays (8). For instance, pores with a minimum diameter of about 1.5 µm were etched with period of 4 µm, while a minimum diameter of about 5 µm was achieved for pores with period of 20 µm. No limitation has been reported for the maximum diameter of feasible pores, although on the basis of experimental outcomes it is likely that a maximum diameter also exists and is probably related to spatial period. A maximum spatial period of 20 µm has been reported to be achievable by

![Figure 2](https://example.com/figure2.png)

**Figure 2.** ECM-fabricated electrically-actuated microstructures and microsystems: (left panel) SEM images, at different magnifications, of a MEMS structure consisting of an inertial, free-standing mass equipped with high-aspect-ratio comb-fingers and suspended by high-aspect-ratio folded (scale bars in b and c) are 50 and 20 µm, respectively; (right panel) SEM images, at different magnifications, of a mechanical microgripper consisting of two fingers electrically actuated by comb-finger batteries driving a spring system, which allows rotation of the two fingers to be performed symmetrically (scale bars in e and f) are 100 and 10 µm, respectively). (After Ref. 18)
ECM for ordered macropore array (8), beyond which either sidewall roughness of etched microstructures was no more accurately controlled or unwanted silicon etching (e.g. formation of random macropores) occurred between adjacent etched features. For certain cases, limitation on the maximum spacing between adjacent etched features can be overcome by making use of sacrificial structures to be removed after switching the etching between anisotropic and isotropic phases at the very end of the process (18). In such a way functional structures with spacing ranging from a few µm up to several mm have been fabricated with high accuracy (18-27). A further possibility for scaling down/up both size and spacing of etched features is reducing/increasing the doping of silicon substrates. A minimum size of 0.3 µm has been reported for ordered macropore arrays with period of 1.5 µm etched on silicon with resistivity of 0.1 Ωcm (3). A maximum size of 42 µm has been reported for ordered macropore arrays with period of 44 µm etched on silicon with resistivity over 2000 Ωcm.

A further limitation of ECM deals with significant reduction of etching rate (already lower than that of TMEP) as the etching depth increases. Although it is feasible to control the etching features over the whole depth of silicon wafer, square root reduction of etching rate with time yields the etching of structures with depth over 400 µm impractical (from several hours to one day) (5, 32). For instance, an etching time of 240 min has been reported for fabrication of 200-µm-deep macropores from which silicon dioxide microneedles with length of 100 µm were produced for transdermal glucose monitoring (19, 27). Increasing HF concentration (typical values are as low as a few percent) allows in principle to speed up the etching up to several tens of µm/min, but the formation of secondary pores arising from unwanted dissolution of sidewall of etched microstructures, a phenomenon known as branching, yields the etching scarcely controlled at high HF concentrations (5).

Figure 3. ECM-fabricated photonic and optofluidic platforms: (left panel) SEM images of a 1DPhC self-powered drop-and-measure platform integrating a 1DPhC, which is exploited as a label-free sensing element operating under capillary-action, in the middle between the optical and fluidic paths (scale bars in b) and c) are 50 µm). (right panel) SEM bird-view picture, at different magnifications, of an all-silicon optical platform integrating five 1D-PhCs featuring a different number of silicon/air elementary cells are integrated (scale bars in b) and c) are 50 and 20 µm, respectively). (After Ref. 26 and 24).
The Future of ECM

Future of ECM will probably depend on the degree to which this technology will meet and satisfy microfabrication needs at industrial level. Besides specific advantages and drawbacks of ECM with respect to TMEP, scaling up of ECM technology to wafer level, from laboratory-scale silicon die with size of 1” (about 25 mm) to industrial-scale silicon wafer with size of 8” (about 200 mm), is certainly a major issue. A single example of ECM-fabrication of ordered macropore arrays with size of 2 µm, period of 5 µm, and depth up to 400 µm on 6” wafer has been successfully reported using a double-thank electrochemical cell able to manage one single wafer (42). Nonetheless, besides macropores, batch parallel fabrication of microstructures on multiple wafers at the same time is highly desirable for industrial manufacturing, so that a specific equipment, besides technological issues, must be engineered to both support and push industrial applications of ECM. To this end, it is worth highlighting that electrochemical processes, equipments, and related technological issues are not novel in microelectronics. As an example, electrodeposition of copper interconnections (developed at IBM in 1990 and known as Damascene process) for integrated circuits (ICs) has now entered mainstream fabrication flow (43). By building on such a former experience, availability of equipments for ECM batch processing at industrial level is reasonably envisaged, so that we could expect to see application of ECM at industrial level in the next few years.

References
