Meso and nanostructured materials are extensively studied in view of their peculiar electrical, optical, and mechanical properties for applications in many fields, from electronics to optoelectronics, from photovoltaics to biomedicine and environment monitoring. Among such materials, mesostructured and nanostructured silicon obtained by low-cost anodization of either p or n-type crystalline silicon, namely porous silicon (PS), has been successfully employed for the fabrication of integrated gas sensors, exploiting the high sensitivity of PS electrical and optical properties to gas and vapor adsorption, and, more recently, for the fabrication of high-efficiency solar cells, exploiting the fine tuning of PS refraction index for producing antireflection coatings and increasing light absorption.

In this work, fabrication, electrical characterization, and modeling of fully porous pn junctions (FPJs) consisting of elemental mesoscopic crystalline junctions operating in parallel, is presented. The proposed approach foresees top-down low-cost fabrication of high-density mesoscopic crystalline pn junctions for both photovoltaic and sensor applications.

The starting material was an n-type silicon substrate ($N_D \approx 10^{15}$ cm$^{-3}$), (100) oriented, with a 4 $\mu$m thick p-type epitaxial layer ($N_A \approx 10^{18}$ cm$^{-3}$) on top. Boron implantation and diffusion were employed to get a shallow, high-doped, $p^+$ layer on top of the low-doped $p$ region. The resulting $p^+n$ diode had a metallurgical junction at the depth of 2.4 $\mu$m. The value of the surface doping concentration ($1 \times 10^{17}$ cm$^{-3}$) was chosen to comply with two opposite needs: on one hand, increasing the surface doping value is desirable to reduce both electrical contact with mesoscopic junctions and series resistance of mesoscopic junctions; on the other hand, very high surface doping value leads (as experimentally verified both for $1 \times 10^{18}$ and $2 \times 10^{19}$ cm$^{-3}$ superficial doping values) to abrupt changes in PS morphology between regions with higher (on top of the $p$ layer) and lower (at the bottom of the $p$ layer) doping concentration, which turns in a partial (or even complete) detachment of the PS top layer due to mechanical stress. FPJs were formed by a single anodization step in aqueous electrolytes containing HF (11% wt.) as well as 1700 ppmv of an apolar surfactant (NCW-1001). A current density of 1 mA/cm$^2$ for 60 min, photogenerated by illuminating the top of the sample with a halogen lamp of 125 W, was used to produce a continuous PS layer across the pn crystalline junction, as shown in Fig. 1. The resulting continuous PS layer is characterized by: (1) high-density mesopores in the $p^+$-type silicon (top); (2) a transition region from higher density mesopores to lower density macropores across the pn junction (middle); (3) lower density macropores (with non-constant depth) in the n-type silicon (bottom). The different PS morphologies resulting from anodization of the pn junction are in agreement with the doping (type and concentration) profile of the anodized crystalline silicon.

An aluminum (Al) film (200 nm thick) was thermally evaporated on top of the PS layer through a metal mask to obtain several circular metal dots (about 7 mm$^2$ each) representing the anode terminals of the different on-chip FPJs. A further Al evaporation on the back-side of the sample (ohmic contact) provided all the on-chip FPJs with a common cathode terminal. The chips were then properly packaged to allow electrical characterization of the different FPJs to be performed.

Electrical characterization of FPJs was carried out at atmospheric pressure and room temperature. Figure 2 shows the typical I-V curves of one of the on-chip FPJs, measured right after chip packaging as well as at different aging times (gray traces). All tested FPJs showed a rectifying behavior, although a small spreading of I-V curves from device-to-device on the same chip is present, with a rectification ratio $RR = \frac{abs[I_{FP}(1V)]}{I_{FP}(-1V)}$ which tends to increase with aging ($RR = 1.65$ after 1 day, 16.05 after 12 days for the
device of Fig. 2). As visible in Fig. 2, a significant reduction of the reverse saturation current \( I_0 \) can be observed with aging, together with a slight reduction of the forward current.

An attempt to model this behavior was made by assuming that a FPJ is formed by a crystalline \( pn \) junction, which accounts for many elemental mesoscopic crystalline junctions connected (in a first approximation) in parallel, with both a series and a shunt resistor, the latter consisting of conduction paths on the surface of each elemental junction. As well known in the literature, as-anodized PS has a positive surface charge due to adsorbed molecules that accounts for silicon mesocrystals depletion and, possibly, for the presence of microscopic conduction path at the surface itself.\(^5,7\) Room temperature oxidation occurring with aging slowly removes conduction path at the surface thus better highlighting the rectifying behavior of FPJs.

To check this hypothesis out, a few FPJ chips were cut in two pieces and a controlled thermal oxidation (\( T = 200 \degree C \) for 1 h in dry \( O_2 \)) was performed on one of the pieces so as to grow a few tens nanometers of silicon dioxide on the PS surface (controlled aging). Figure 2 shows the typical \( I-V \) curves of FPJs after thermal oxidation, measured right after chip oxidation as well as at different aging times (black traces)\.\(^{11}\) Thermal-oxidized (Ox) FPJs show a significantly higher rectifying behavior (\( RR = 362.3 \) after 1 day, 2712.7 after 12 days for the device of Fig. 2) with respect to as-fabricated (NoOx) FPJs. Moreover, conversely to NoOx-FPJs, \( I-V \) curves of Ox-FPJs only slightly change with aging time. For instance, as-fabricated FPJs shows a large absolute variation of both forward and reverse current over 12 days of storage in air at room temperature, e.g., \( \Delta I_{FPJ}(+1V) = 2.82 \mu A \) and \( \Delta I_{FPJ}(-1V) = 3.53 \mu A \) for the NoOx-FPJ of Fig. 2; on the other hand, thermal-oxidized FPJs show a smaller aging induced current variation over the same aging time, e.g., \( \Delta I_{FPJ}(+1V) = 10 \mu A \) and \( \Delta I_{FPJ}(-1V) = 10 \mu A \) for the Ox-FPJ of Fig. 2. The small residual aging effect on Ox-FPJs is mainly visible for reverse polarization.

In order to extract the electrical parameters of FPJs, the \( I-V \) curve of the diode was analytically modeled according to Eq. (1),\(^{12}\) which takes into account space-charge and quasi-neutral region generation/recombination phenomena as well as shunt and series resistances \( R_s \) and \( R_p \), respectively:

\[
I = \frac{V}{R_p} + I_1 \cdot \left[ e^{\beta_1 V} - 1 \right] + I_2 \cdot \left[ e^{\beta_2 (V - R_s I) / R_s} - 1 \right],
\]

where \( I_{1,2} \) are two terms contributing to the junction saturation current, and \( \beta_1,2 = q / (\eta_{1,2} \cdot k \cdot T) \), with \( \eta_{1,2} \) ideality factors. It must be noted that the effect of the series resistance \( R_s \) was supposed to significantly affect only the second exponential function, which represents the high-current region of the \( I-V \) curve. The Lambert W (LW) function was employed to obtain for the transcendental Eq. (1) an explicit analytical solution:\(^{13}\)

\[
I = \frac{1}{\beta_e R_s} \text{LW} \left\{ \beta_s R_s I_2 e^{\beta_1 V} e^{-\beta_s R_s [(V/R_s) + I_1 (e^{\beta_1 V} - 1) - I_1]} \right\} \\
+ \frac{V}{R_p} + I_1 (e^{\beta_1 V} - 1) - I_2,
\]

that can be better exploited to perform the best-fitting of experimental data by using \( I_1, I_2, R_s, R_p \) as fitting parameters.

Best-fitting of the as-fabricated FPJ experimental \( I-V \) curves of Fig. 2, measured over an aging time of 2 weeks, highlighted (1) a significant decrease (a few order of magnitudes) of both \( I_1 \) (from \( 3 \times 10^{-4} \) to \( 2.7 \times 10^{-7} \) A) and \( I_2 \) (from \( 1.3 \times 10^{-4} \) to \( 5.8 \times 10^{-6} \) A); (2) a nearly constant value of the series resistance \( R_s \approx 300–400 \Omega \); (3) a large increase (over 1 order of magnitude) of the shunt resistance \( R_p \) value (from 460 to 7400 \( \Omega \)). For the thermal-oxidized FPJ experimental \( I-V \) curves of Fig. 2 the best-fitting procedure resulted in (1) a nearly constant value for \( I_1 \approx 1.2 \times 10^{-6} \) A and \( I_2 \approx 1.1 \times 10^{-6} \) A, which is consistent with the behavior of aged NoOx FPJs; (2) \( R_s \approx 60 \Omega \), which is smaller than that of NoOx-FPJs and compatible with the annealing effect on Al contacts (front and back) due to the thermal treatment; (3) a significant increase of the shunt resistance \( R_p \) value (from \( 7.87 \times 10^4 \) to \( 6.21 \times 10^7 \) \( \Omega \)), which is always significantly larger than that of NoOx-FPJs and indicates the better passivation, although not yet complete, of the PS surface due to
thermal treatment with respect to room temperature oxidation. The theoretical $I$-$V$ curves (dotted traces) obtained from the best-fitting procedure ($\text{RMSE} = 8.8 \times 10^{-8}$ for Ox-FPJ, $\text{RMSE} = 2.6 \times 10^{-6}$ for the NoOx-FPJ) of experimental $I$-$V$ curves (solid traces) measured after an aging time of 12 days are reported in Fig. 3, both for the as-fabricated and thermal-oxidized FPJs.

On the basis of the above-reported theoretical analysis, the rectifying behavior of FPJs is compatible with elemental mesoscopic $pn$ crystalline junctions resulting from anodization of a macroscopic $pn$ silicon junction and operating in parallel. Rectifying effects at the Al/PS interface, which could be in principle also responsible of the observed effects, can be ruled out on the basis of electrical measurements performed on free-standing Al/PS/Al membranes, which always showed an ohmic $I$-$V$ characteristic.\textsuperscript{14}

In this work, a top-down low-cost approach for fabricating fully porous $pn$ junctions (FPJs) was proposed. Electrical characterization and analytical modeling demonstrate that each FPJ consists of high-density randomly distributed mesoscopic crystalline $pn$ junctions operating in parallel. Further work is in progress for controlling the etching process so as to produce a regular array of high-density mesoscopic $pn$ junctions operating in parallel for sensing and photovoltaic applications.

11. $I$-$V$ curves reported in Fig. 2 for as-anodized (gray traces) and thermal-oxidized (black traces) FPJs were measured on non-oxidized half and thermal-oxidized half of the same chip, respectively.