Electrochemical etching of silicon in hydrofluoric acid (HF) electrolyte is a well known technique for the formation of porous silicon. The fabrication of macropores in crystalline silicon by photoelectrochemical etching in a hydrofluoric acid electrolyte is investigated. It is shown that the dimensional constraints on the pore diameters, which, in previous literature, are considered to depend on substrate doping, can be significantly relaxed. We show that it is possible to fabricate arrays of square section macro pores with sides ranging from 2 to 15 μm using the same n-doped (2.4-4 Ω cm) silicon substrate. Moreover, we demonstrate that macropore arrays with pitch variation up to 100% (8 and 16 μm) can be simultaneously grown on the same sample. The same process is used to fabricate arrays of silicon walls with different spacing and pitch as well. A simple model, based on the coalescence in a single pore of multiple stable pores, is proposed to explain the experimental data.

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E-mail: g.barillaro@ing.unipi.it
The macropore average diameter has been estimated by scanning electron microscope (SEM) observations in about 2 μm, in agreement with the literature data. The same silicon substrate was used to fabricate regular high aspect ratio structures, following the fabrication process sketched in Fig. 3. A silicon dioxide layer (5000 Å thick) was grown on the sample by thermal oxidation (Fig. 3a). A pattern was defined using a standard photolithographic process. The patterns were arrays of square holes of different side and pitch, and arrays of straight lines with different width and pitch. Some of the studied dimensions are summarized in the first column of Tables I and II. A buffered hydrofluoric acid (BHF) etch was then used to transfer the pattern to the silicon dioxide (Fig. 3b). Pyramidal notches were created by KOH etching through the patterned silicon dioxide (Fig. 3c). Electrochemical etching in HF was then used to fabricate regular structures in the silicon substrate (Fig. 3d), using the above described electrochemical cell. The last step of the process was a drying one, performed in air at 95°C for 10 min. The fabricated samples were finally cleaved to allow SEM observations of the cross sections.

### Results and Discussion

Patterned pores with sides ranging from 2 μm up to 15 μm were fabricated starting with the aforementioned silicon substrate, using the above detailed process. The sample porosity was changed between 25 and 90%, starting with a fixed initial pattern and only varying the etching current. In Fig. 4 an SEM cross section of a square hole array with pitch of 16 μm having pores with side of 15 μm, corresponding to 90% of porosity, is shown. Macropores are about 35 μm deep, corresponding to 20 min of etching time.

The porosity \( p \) of the array, defined as the ratio between the volume of etched silicon and the total initial volume, is determined, at the steady state, by the etching current density \( J \) according to the relation \( p = J/J_{ps} \), where \( J_{ps} \) is the critical current density at the pore tips. Varying the etching current density is then a viable way to control the porosity of the sample under etching. Consequently,
starting with the same initial pattern, it is possible to change the geometrical dimensions of the pores. Indeed, for an orthogonal pattern of square holes with pitch \( r \), where the pitch is defined as the period of the pattern, the pore side \( s \) is, from simple geometrical considerations, \( s = r \sqrt{2} \).

In Table I some of the fabricated structures are summarized. For each row, we report in the first column of the table the KOH starting pattern (shape and geometrical dimensions of pattern before the anodization process) and in the next columns the porosity values obtained for the fabricated samples. In the table we indicate with an \( X \) the patterns obtained without any defect, while the \( B \) indicates samples in which branching of the pores occur; finally, the “solidus” character means that the sample cannot be fabricated with the specified porosity value (as is clarified below). For instance, in the last row of the table we can see that starting from an initial KOH squared hole array with \( 8 \mu \text{m} \) side and \( 16 \mu \text{m} \) pitch, it is possible to vary the porosity of the anodized sample from \( 50 \) to \( 90 \% \), using a proper etching current. No branching of primary pores is observed for the above specified porosity. It must be noted that, in the above example, a value of porosity of \( 90 \% \) corresponds to pores with sides of \( 15 \mu \text{m} \), while the width of the silicon walls between two adjacent pores is \( 1 \mu \text{m} \). When the porosity is \( 25 \% \) or lower, branching of primary pores is observed in the silicon wall separating pores. For a \( 25 \% \) porosity, the initial pattern was simply transferred to the silicon substrate; the side of pores and the wall thickness between the adjacent pores of anodized sample remains \( 8 \mu \text{m} \) as in the mask. In order to explain the use of the solidus character we observe that, due to the fact that the average diameter of the random pores is about \( 2 \mu \text{m} \) for the used substrate, it is not possible to fabricate samples with porosity requiring pores with diameters less than \( 2 \mu \text{m} \). This is, for instance, the case reported in Table I for a porosity \( < 25 \% \) with starting pattern \( 2 \mu \text{m} \) side, \( 4 \mu \text{m} \) pitch square hole array.

No limit for upper porosity is found in our samples. As matter of fact, branch-free, regular macropore arrays with porosity up to \( 90 \% \) were fabricated (see Table I). On the contrary, it is evident from Table I that a porosity lower limit exists. Below the lower porosity limit secondary pores, \( \langle 100 \rangle \) oriented, grow in the silicon walls separating the primary ones. This effect was explained by considering the width of the walls separating neighboring primary pores. It is commonly accepted\(^1\) that the macropore growth process is ruled by the extension of the space charge region around the pore tips, so that when the wall width between neighboring pores is about twice that of the space-charge region, too few holes penetrate in the silicon wall to promote silicon dissolution, and no pores grow in the silicon between adjacent ones. On the contrary, when the wall thickness becomes wider, more holes, generated deep in the substrate, can diffuse into the silicon walls and reach the Si-HF interface, where they react with the electrolyte giving rise to the growth of secondary pores.

The space-charge region width \( w \) for the electrochemical system under investigation can be estimated from the Schottky contact theory\(^1\),

\[
w \approx \left( \frac{2 e e_0 V_j}{e N_D} \right)^{1/2},
\]

with \( e \) and \( e_0 \), respectively, the dielectric constant of Si and the vacuum permittivity, \( V_j \) junction voltage, \( e \) elementary charge, and \( N_D \) the concentration of donors. All the experiments were performed with an anodization voltage of \( 3 \) V; assuming that all the voltage drops at the silicon-electrolyte interface, we obtain an excess estimation of \( w \) ranging between \( 1.4 \) and \( 1.7 \mu \text{m} \) for the silicon substrate doping we used. In our samples, branching of primary pores is observed when the wall thickness between near pores is greater than \( 4 \mu \text{m} \), which is more than twice that of the space-charge width. This result does not completely agree with the predictions for macropores formation in n-type silicon which are based on the aforementioned space-charge region model. Results in agreement with our experiments were reported by Foll et al.\(^15\) for random macropores in a silicon wafer with the same orientation and similar resistivity. This fact seems to suggest that hole diffusion in the substrate is probably the main limiting effect for pore branching, but other phenomena should also be considered in order to properly model the pore branching, for instance, the ohmic resistance in the narrow non-depleted region between adjacent pores could play a role as well.

The experimental data suggest that for macropore array fabrication, once the substrate resistivity is fixed, no higher limit exists for porosity; any increase of it simply results in larger pores and thinner walls separating pores. A limit was found, however, for the thickness of the silicon walls separating adjacent pores. In fact, once the initial pattern is given, a minimum value always exists for the porosity of the macropore array, corresponding to a maximum width for the silicon wall separating pores. Below this porosity limit it is not possible to fabricate branch-free patterned pores.

Arrays with different dimensions can be grown on the same silicon sample, once the porosity (that is, the etching current density) has been chosen. Two different patterns with a \( 100 \% \) pitch variation were fabricated on the same sample; an SEM top view is shown in Fig. 5. The initial pattern in the oxide was constituted by two arrays, \( 4 \mu \text{m} \) squares with a pitch of \( 8 \mu \text{m} \), and \( 8 \mu \text{m} \) squares with a pitch of \( 14 \mu \text{m} \).

### Table I. Condition of fabricated macropore arrays for different dimensions and porosities. An X means a flawless sample, a B means lateral branching, while “/” means a sample that cannot be fabricated (see text).

<table>
<thead>
<tr>
<th>Hole square array</th>
<th>Porosity</th>
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<tbody>
<tr>
<td></td>
<td>&lt;25%</td>
</tr>
<tr>
<td>2 μm pitch 4 μm</td>
<td>/</td>
</tr>
<tr>
<td>4 μm pitch 8 μm</td>
<td>X</td>
</tr>
<tr>
<td>8 μm pitch 16 μm</td>
<td>X</td>
</tr>
</tbody>
</table>

\( B \) indicates samples that were impossible to fabricate because of the mask design. For instance, the case reported in Table I for a porosity \( < 25 \% \) with starting pattern \( 2 \mu \text{m} \) side, \( 4 \mu \text{m} \) pitch square hole array.

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**Figure 5.** SEM top view of two difference macropore arrays with 100% pitch variation. A macropore array with 14 μm side and 16 μm pitch (left) was fabricated simultaneously with an array with 7 μm side and 8 μm pitch (right). Random macropores present in the area between the arrays were destroyed by the drying step.
of 16 μm. With a proper choice of the current, a pore array with a 14 μm side and a 16 μm pitch (Fig. 5, left) and an array with a 7 μm side and a 8 μm pitch (Fig. 5, right) were simultaneously fabricated. A SEM cross section of the Fig. 5 left array is shown in Fig. 6. Pores shown in Fig. 5 and 6 are 35 μm deep, corresponding to 20 min of etching time with 27 mA/cm² etching current density. Interestingly, the obtained porosity is greater than that of the initial pattern (25%) for both arrays, and it is found to be about 75% in both arrays, in agreement with the current density used in the experiment. It must be noted that the abrupt end of the pattern does not lead to branching of pores.

Wall arrays were also fabricated, using KOH patterned straight lines as initial nucleation sites for electrochemical silicon etching. Dimensions and porosity of the fabricated structures are summarized in Table II, in a similar manner to the macropores case of Table I. Again, no limit is found for higher porosity. However, as in the case of macropore arrays, a lower limit exists, but it is clear from Table II that the maximum allowable width of silicon walls is significantly greater (up to 6 μm) than the maximum width in square arrays. This could be explained by considering the field effect of corner existing in the macropore arrays between four neighboring pores. In fact, in the wall array no angles exist focusing electric field lines, so that a reduced number of holes, coming from the substrate, are present in the silicon walls, due to insignificant drift field effect. So, it should be again considered that not only the space-charge layer, but also hole path resistance and geometrical shape of the fabricated structures could influence the thickness of the silicon walls in the electrochemical etching and thus the lower limit of the porosity. A SEM cross section of a wall array is shown in Fig. 7. The array was obtained by the anodizing of a KOH pattern of 4 μm wide straight lines with a pitch of 8 μm. Thickness of the walls is about 2 μm, while the spacing is 6 μm, corresponding to 75% porosity, according to the current density used in the experiment. The walls are about 25 μm deep.

The above reported experimental results do not completely agree with the commonly accepted limits reported in Ref. 12. As already pointed out, the theoretical relationship concerning porosity and pore diameter only depends on the etching current density; however, in Ref. 12 the substrate resistivity was found to be crucial for the pore diameter. This is reasonable when the macropore growth process is supposed to depend only on the extension of the space-charge region at the pore tips. In fact, if the stable pore diameter reduces with the depletion region width, which in turn depends on the doping density of the substrate, a misadjustment of pitch and/or doping density leads to branching of pores for high doping densities or to dying pores for low doping densities. The region of stable pore diameters is, then, a narrow function of the substrate resistivity. On the basis of their results the sensitivity of the system to small varia-

<table>
<thead>
<tr>
<th>Wall array</th>
<th>Porosity</th>
</tr>
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<tbody>
<tr>
<td>2 μm pitch 4 μm</td>
<td>&lt;25%</td>
</tr>
<tr>
<td>4 μm pitch 8 μm</td>
<td>B</td>
</tr>
<tr>
<td>8 μm pitch 16 μm</td>
<td>B</td>
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</table>

Table II. Condition of fabricated wall arrays for different dimensions and porosities. For the meaning of symbols refer to Table I.
tions of pitch or doping (for instance, a reduction of the pitch by only 3%) should change a perfect pore pattern to an imperfect one. A rule of thumb for selection of silicon substrate was given, i.e., the square of the desired pore diameter (in micrometers) gives the appropriate substrates resistivity (in ohms per centimeter). For example, 2 μm pores could be growth only using a 4 Ω cm n-type substrate, and it should not be feasible to fabricate regular macropore array with a side up to 15 μm using our substrate. Moreover, the fabrication of regular macropore array with a pitch variation of about 100% should not be possible.

On the basis of exhaustive SEM investigation of the fabricated structures, we suggest a macropore growth model which is able to explain our experimental results. It is known that stable random macropore growth on surfaces without prestructured nucleation sites is preceded by two phases of pore nucleation and redistribution.15 We suggest that the same nucleation and redistribution phases still exists for stable macropore growth also on prestructured silicon surface. Moreover, we postulate that the phase of pore redistribution is a crucial step for HF electrochemical silicon etching. The evolution model for HF electrochemical silicon regular macropore formation process is schematically shown in Fig. 8. For the first time, shallow macropores are formed in correspondence to pre-existing defect sites (Fig. 8a and b). The surface density of the shallow macropores could be relatively high, about the defect density of a polished silicon surface (10⁶ defects/cm²). When the silicon between neighbor-

Figure 8. Schematic steps of time evolution model for HF electrochemical silicon etching (macropore formation).

Figure 9. SEM cross sections of two wall arrays fabricated starting with 2 μm straight lines and a pitch of 4 μm, and different current densities. The width of the initial notch is close to the diameter of stable pores. At 50% porosity (top), corresponding to 2 μm pores and walls, a single pore grows at each site, while at 90% porosity (bottom), corresponding to 0.4 μm pores and 3.6 μm walls, two pores grow at each site.
cantily change anymore (Fig. 8e and f). The overall structure grows deep without further modification of dimensions and shape.

Interestingly, the number of pores growing in the predetermined notch depends on its dimensions. If the typical dimension of the notch is approaching the diameter of stable random pores, only one pore grows in correspondence of the single defect, as reported by the commonly accepted model for macropore formation.\(^8\) When the dimension of the defect is much greater than the diameter of the random pores, more pores grow in the defect site and coalesce, creating a structure with a greater dimension. For instance, a 2 \(\mu\)m pitch, 4 \(\mu\)m square array was fabricated with only one macropore growing at each pyramidal notch, while a 4 \(\mu\)m pitch, 8 \(\mu\)m square array was fabricated with four macropores growing and joining in each site. In both the experiments, it was necessary to hold the etching density current at 0.25 \(J_{\text{ps}}\), corresponding to 25\% of porosity, in order to fabricate a pore array having the same geometrical dimensions as the initial KOH pattern. In fact, we found that the number of stable pores growing into a single prepatterned defect depends also on the initial KOH pattern. In this paper a study of the photoelectrochemical formation of prepatterned macropores on a silicon substrate with 2.4-4 \(\Omega\) cm resistivity is reported. Dimensional constraints for macropore dimensions as a function of the resistivity of the substrate are shown to be significantly less severe than those reported in the previous literature. Macropore arrays with sides ranging between 2 and 15 \(\mu\)m, as well as arrays of walls with comparable dimensions, were fabricated on the same substrate. A simple physical model based on the coalescence of several smaller random pores, which includes the commonly accepted model as a particular case, is proposed to explain the experimental data. This increased flexibility in the choice of the dimensions could allow new applications of the photoelectrochemical etching technique in the field of silicon microfabrication.

### Conclusions

In this paper a study of the photoelectrochemical formation of prepatterned macropores on a silicon substrate with 2.4-4 \(\Omega\) cm resistivity is reported. Dimensional constraints for macropore dimensions as a function of the resistivity of the substrate are shown to be significantly less severe than those reported in the previous literature. Macropore arrays with sides ranging between 2 and 15 \(\mu\)m, as well as arrays of walls with comparable dimensions, were fabricated on the same substrate. A simple physical model based on the coalescence of several smaller random pores, which includes the commonly accepted model as a particular case, is proposed to explain the experimental data. This increased flexibility in the choice of the dimensions could allow new applications of the photoelectrochemical etching technique in the field of silicon microfabrication.

### References