A porous silicon LED based on a standard BCD technology

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Abstract

A new process, compatible with an industrial Bipolar + CMOS + DMOS (BCD) technology, has been developed for the fabrication of efficient porous silicon based LEDs. The electrical contact is fabricated using a n+ polysilicon layer on double n+/p implant before the porous silicon (PoSi) formation, achieving a high current injection. The anodisation is performed as the last step of the process, thus reducing potential incompatibilities with industrial processes. The fabricated devices show yellow–orange electroluminescence (EL), visible with the naked eye. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

Porous silicon (PoSi) based LED’s are a subject of great interest, in view of a possible integration of silicon optoelectronic devices with standard silicon circuits. Two fundamental problems must be solved: the compatibility of the fabrication process with the integrated circuit industrial processes and the light emission efficiency. In present LEDs, the overall efficiency is severely reduced because of the very low current injection efficiency into the porous layer, even when the internal quantum efficiency (IQE) is high. As a matter of fact, in both Schottky-like and p–n junction devices [1,2] charge carrier injection is inefficient due to the low quality of the interface between the injecting contact and the PoSi. This interface is formed by depositing a thin conducting film (metal or polysilicon) directly onto the PoSi, after the porisation has taken place. Any subsequent thermal step that could improve the electrical characteristics of the interface cannot be easily performed because of the sensitivity of PoSi luminescence to thermal treatments.

In an effort to solve these problems, a PoSi-based n+–p junction LED was designed and fabricated. The current injector is a polysilicon n+ film on top of a n+-doped crystalline silicon region. The electrical contacts are fabricated before the porous layer formation and the need for subsequent technological steps is therefore eliminated, with the mentioned advantages in terms of electrical properties of the device. Moreover, a graded p doping under the n+ contact, a technique first proposed for micromachining applications [3], avoids an incomplete anodisation under the contact; in this way, all the injected current is forced through the PoSi layer, and an improvement in light emission efficiency is expected. In this paper
the fabrication process and the preliminary measurements are presented.

2. Fabrication process and results

The fabrication process of the LED structures is based on an industrial BCD process and schematically consists of the following steps: (1) wet oxidation (about 90 nm) of a p type (100) wafer with a doping of $10^{15}$ cm$^{-3}$; (2) boron implantation (implantation energy: 70 keV, implantation dose: $2.8 \times 10^{13}$ cm$^{-2}$) through the oxide to create a grid-like pattern, 1.4 μm deep, with an higher p doping (pBody); grid lines are 4 μm wide and several hundreds microns long (Fig. 1(a)); (3) arsenic implantation (implantation energy: 50 keV, implantation dose: $5 \times 10^{15}$ cm$^{-2}$) to define an n$^+$ contact 0.23μm deep on the pBody lines (Fig. 1(b)); (4) polysilicon deposition (450 nm) and polysilicon n$^+$ implantation; (5) polysilicon patterning to define the front contact (constituted by a poly/SiO$_2$ structure) and the lines to the active (luminescent) area (Fig. 1(c)); (6) deposition of an LPCVD Si$_3$N$_4$ layer with a thickness of 90 nm; this film acts as a masking layer during the anodisation process, as will be clear later; (7) deposition of an spinnable SiO$_2$ (TEOS) layer (500 nm), to be used as a mask for the Si$_3$N$_4$ etching (Fig. 1(d)); (8) definition of a window onto the SiO$_2$ to expose the active area; (9) wet Si$_3$N$_4$ etching by means of an H$_3$PO$_4$ solution and (10) etch of the residual oxide (Fig. 1(e)). The final step was the selective anodisation of the structure through the Si$_3$N$_4$ window (Fig. 1(f)).

The anodisation process, performed in the dark, acts only on p doped silicon, whereas the n$^+$ poly/n$^+$ silicon are not affected [4]. In this way a p PoSi layer is formed and the n$^+$ poly/n$^+$ silicon contact is left unchanged, so that the fabrication of an electrical contact on PoSi after its formation is unnecessary. The composition of the solution was 1:1 (vol.) HF (48%):C$_2$H$_5$OH (99.9%). After the anodisation the samples were rinsed in ethanol and pentane and dried in nitrogen ambient.

Since the PoSi formation occurs along anodisation current paths, if the doping of the p silicon is uniform under the n$^+$ contact a crystalline pillar is not affected by the porisation process. In our structures, the presence of a graded p doping forces the anodisation current under the n$^+$ contact: when the border of the anodized (porous) volume reaches the highly doped p region, the current lines bend under the contact, and the anodisation proceeds at a higher rate in that area. Fig. 2 (a)
and (b) shows scanning electron microscope (SEM) images of a cross-section of two structures anodized for 120 and 180 s, respectively (current is 25 mA/cm² in both cases). The formation of the buried layer can be monitored by measuring the driving anodisation voltage, which decreases when the pBody region is reached, and increases when this region becomes fully porous.

The choice of anodisation parameters (current and time) is critical in several respects: higher current densities imply higher porosity and better quantum efficiency of light emission [5], but a more brittle material; moreover, the formation of the continuous buried PoSi layer is also influenced. For instance, the buried layer was obtained both with 25 mA/cm² for 3 min, and with 5 mA/cm² for 15 min. Though a poly/SiO₂ multilayer is claimed to be a mask for the anodisation process [6] the SiO₂ layer under the poly is etched during the anodisation, an effect probably caused by diffusion of reactants through the poly layer. Higher currents reduce, but do not eliminate this problem.

Structures with various anodisation parameters show light emission, visible with the naked eye, both with forward and reverse polarization. Typical polarization conditions for reverse luminescence are 10 mA at 40 V for a square device 1600 × 1600 μm² in size; the luminescence, white in color, is confined in a narrow area around the pad and contact strips. A very similar behavior has already been observed by other groups [7], and attributed to recombination of hot carriers under breakdown conditions. Visible yellow–orange electroluminescence (EL) is obtained with 15 mA at 15 V for the same device, but is confined along the polysilicon lines connecting the pad with the poly grid. A typical I–V curve of fabricated devices is shown in Fig. 3. Such behavior was attributed to the non-uniform current injection, probably due to the aforementioned damage of the polysilicon strips, confirmed by SEM observations, and should be solved with a better tuning of the anodisation parameters. Preliminary EL spectra show a broad lineshape (~200 nm) peaked at 750 nm wavelength. The integrated EL grows linearly with the current. Further details will be published later.

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**References**