Fabrication of self-aligned gated silicon microtip array using electrochemical silicon etching

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In this paper we report a new approach to fabricate gated silicon microtip arrays for field emission applications using a single mask process. The key role in the fabrication process is played by the photoelectrochemical etching of silicon in HF-based electrolytes. This technique is here exploited to produce highly uniform silicon microtip arrays. The fabrication process is detailed and the dependence of the tip geometry on the electrochemical etching parameters is discussed.

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1 Introduction

Integrated silicon microtip arrays have been investigated for vacuum microelectronic applications, such as field emission displays (FEDs) and microwave devices [1]. Many different materials and structures have been proposed for fabrication of microtip arrays, though several problems, uniformity and reproducibility at first, still exist. Metal tips evaporation into a trench was first reported by Spindt (Spindt-type emitters) [2]; crystal silicon tips formation by isotropic [3] or anisotropic [4] chemical silicon etching were also proposed. Typical fabrication process of a silicon field emitter array consists of tip fabrication by silicon etching, evaporation or growth of gate oxide, deposition of metal gate and lift-off of the gate insulator to uncover the silicon tip.

Electrochemical silicon etching in HF-based electrolytes is a well known technique for porous silicon formation [5]. Depending on the silicon doping, on the type of the anodized substrate and on the etching parameters, different pore morphologies can be obtained. Microporous layers, characterized by randomly distributed pores with nanometric dimensions, can be easily grown on p-type substrates, while macro-porous layers with micrometric straight pores can be obtained from illuminated n-type substrates (photo-electrochemical etching) [6]. In the latter, by illuminating the back surface of the wafer electron–hole pairs can be generated in the substrate. Under anodic biasing conditions, the photogenerated holes move to the front surface and silicon dissolution takes place at defect points. Surface defects therefore act as seeding points for macropore formation. By pre-patternning the wafer surface with defect sites it is possible to determine where macropores will grow. KOH etching after a standard photolithographic step is typically used to create inverse pyramidal notches in the required positions which can act as an array of defects. The macropore morphology significantly depends on the anodization conditions, such as current density, etching time, HF concentration, temperature and bias, as well as on substrate properties, such as doping and orientation. Randomly distributed [7] and pre-patterned [8] macropore arrays were grown throughout the thickness [9] and on the whole surface [10] of the wafer with pore ranging from 2 µm to 15 µm [11].

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In this paper, a new fabrication process for gated silicon field emitter arrays is presented. The fabrication process is based on the silicon photoelectrochemical etching in HF-based electrolytes. For the first time, we have successfully used this technique to produce very regular silicon tip arrays with high aspect ratio (tip height/tip width ratio). It has been verified that the process can be used to fabricate silicon microtip arrays with self-aligned chromium metal gates using only one mask.

2 Fabrication process

The fabrication process of the microtip array is schematically shown in Fig. 1. The starting material is a n-type silicon wafer, \( \langle 100 \rangle \) oriented, with \((2.4 \div 4) \, \Omega \, \text{cm}\) resistivity, single side polished, 550 \(\mu\)m thick. A 2000 \(\AA\) thick oxide layer is thermally grown on the samples. Several patterns are defined on the oxide layer using a standard photolithographic process and Buffered HF (BHF) etch (Fig. 1a). Dimensions of pattern in Fig. 1a are: inner square side 1 \(\mu\)m; outer square side 4 \(\mu\)m; pitch 6 \(\mu\)m. The inner square in Fig. 1a determines the position of the tip. A KOH etching is then used to transfer the pattern to the silicon so producing on the substrate an array of notches which is used as a seed for photoelectrochemical silicon etching (Fig. 1b).

Photoelectrochemical etching in a HF-based solution is then performed and the tips are fabricated. Indeed, as macropores only grow and join in the notches, a crystalline silicon tip is left in the center, as will be clarified in the next section (Fig. 1c). At this stage, a typical sample appears as in Fig. 2. As the first oxide is completely removed by HF during the electrochemical etch step, a new thermal oxidation step is then performed to grow a 2000 \(\AA\) thick layer that will constitute the gate insulator. This step also reduces the microtip radius. A chromium metal gate (2000 \(\AA\) thick) is deposited on the silicon dioxide by e-beam evaporation (Fig. 1d). The last step is the metal cap lift-off, which uncovers the silicon tips (Fig. 1e). SEM photographs of a tip after the last step are shown in Fig. 3. The tip radius can be estimated from SEM images to be around 16 \(\text{nm}\).

The experimental setup used for photoelectrochemical silicon etching is constituted of an electrochemical cell made of PTFE (Polytetrafluoroethylene) having a volume of 400 \(\text{cm}^3\). The front side of the silicon sample is in contact with the electrolyte solution. The electrolyte composition is 1:2:17 (vol.) HF(48%):\(\text{C}_2\text{H}_5\text{OH}\)(99.9%):\(\text{H}_2\text{O}\). Ethanol is added to reduce hydrogen bubbles formation at the sample surface, a commonly used technique for microporous silicon formation. For the same reason, the solution is stirred during the anodization process. The area of the sample exposed to the electrolyte solution is about 0.6 \(\text{cm}^2\) and has a circular shape. Electron–hole pairs are generated by illuminating the back side...
of the sample with a 300 W halogen lamp, placed about 15 cm apart from the sample, through a circular window in the aluminum disc used to provide the electrical contact to the sample. The power supply of the lamp can be varied to modulate the etching photocurrent. The counter electrode is a platinum wire immersed into the electrolyte, close to the sample surface (about 5 mm). An HP4145B parameter analyzer is used to apply the anodization voltage and to monitor the etching current. All the experiments are executed at room temperature.

3 Experimental results and discussion

The key role of the silicon field emitter array fabrication described above is played by the photoelectrochemical silicon etching for microtips formation.

In our previous works [11, 12], we proposed that the macropore formation process in silicon electrode is constituted of three phases: i) a nucleation phase; ii) a redistribution phase; iii) a stable growth phase. In the latter phase, the diameter of pores is fixed to a proper value which depends on the substrate resistivity (stable diameter) and it is about 2 µm for the substrate used in this work. Moreover, depending on the dimension of the defined KOH defects and on the etching current density, the number of pores growing at any pyramidal notch can range from a single one to several ones. As a matter of fact, if the dimen-

Fig. 2 SEM top view (left) and cross-section (right) of a silicon microtip array fabricated by using electrochemical etching in HF-based electrolytes (before oxidation step).

Fig. 3 SEM view (left) and zoom (right) of a silicon tip with its chromium gate (after metal cap lift-off).
Effect of initial pattern on the photoelectrochemical etching of silicon in HF-based solutions.

The dimension of the KOH defect is close to the stable diameter of pores (i.e. 2 \( \mu \text{m} \)), only one pore grows at any notch (Fig. 4a), but if the dimension of the defect is larger (i.e. 4 \( \mu \text{m} \) or larger), several pores grow and join at any notch to build a structure with greater dimension (Fig. 4b). A similar effect takes place when the etching current density is raised, once the dimension of defect is chosen (compare Figs. 4a, c). Once the dimension of the initial defect and the etching current are chosen, we found that the overall structure depends on the KOH etching time. For instance, if KOH etching of initial pattern is not complete (truncated pyramid), pores grow at the corners of each defect, where most of holes coming from the substrate are collected due to the higher electric field and, depending on its dimensions and on the etching current, they grow independently or coalesce leaving a silicon pillar in the center of the structure (Fig. 4d). The latter effect is due to the depletion of holes in the pillar: the space charge region in the silicon at the HF-silicon interface of growing pores extends into the pillar, effectively protecting it against silicon dissolution. This is a feasible way to obtain silicon microtips \[13\], but two drawbacks have to be highlighted for field emitter fabrication: 1) the tip position is not easily controlled due to the fact that its location strongly depends on the arrangement of pores growing in the defect; 2) the tip is lower than the silicon surface because of the KOH etching. These effects could act on the field emitter array properties: the former on the uniformity of electrons emission; the latter on the emission voltage threshold, due to the large gate-to-tip distance. Both these drawbacks can be solved by using a defect as in Fig. 4e. In fact, pores will grow in the pre-defined KOH pyramidal notches so that the position of the tip is well defined. Moreover, the tip is as high as the substrate surface, after the electrochemical etching.

High lateral (parallel to the wafer surface) and vertical (perpendicular to the wafer surface) uniformity is obtained, because of the negative feedback ruling the macro pores formation in HF-based solutions \[9, 10\]. Furthermore, as the etching process is an electrochemical etching, high reproducibility of fabricated structures is ensured once the etching parameters (voltage, current density, etc.) are chosen. Moreover, given the geometry of the initial pattern, the dimension of the microtips can be controlled by independently tuning the etching parameters: the etching time acts on the height of the tip, while the current density controls the overall porosity (i.e. the ratio between the etched volume and the total volume of silicon) of the fabricated structure, and consequently, the lateral gate-to-tip distance. Silicon microtips with aspect ratio as high as 50 and over can be obtained with the proposed process.

### 4 Conclusions

In this paper a new process for gated silicon microtip array fabrication for field emission applications has been proposed. Highly uniform silicon microtips have been fabricated by exploiting photoelectrochemical etching of silicon in HF-based electrolytes. It has been demonstrated that the process can be used to fabricate silicon microtip arrays with self-aligned chromium gates using only one mask.
References