A thick silicon dioxide fabrication process based on electrochemical trenching of silicon

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Abstract

Thick silicon dioxide films have recently been proposed for sensor applications (thermal isolation in high-temperature sensors, gas sensors, etc.). In this paper a simple and low cost method to produce thick silicon dioxide layers (thickness of several tens of microns) is reported. The process is based on the photoelectrochemical etching of silicon in HF solution. This technique is here used to produce deep high aspect ratio regular trenches, which are then completely oxidized to obtain a thick silicon dioxide layer.

Keywords: Thick silicon dioxide; Electrochemical etching; Porous silicon; Macropore formation

1. Introduction

Silicon dioxide is a key material both for microelectronic and sensor technologies because of its electrical, thermal, mechanical and chemical properties. Very thick (10–100 μm) silicon dioxide has been recently demonstrated to be a suitable layer for several applications: thermal isolation in microsystems fabrication (gas flow sensors [1,2], thermopiles [3], biomedical sensors [4], gas sensors [5], etc.), passive components integration in RF applications [6], silicon integrated waveguides production in optical interconnections [7]. Although others approaches have also been proposed (bulk micromachining [8], polyimide layers deposition [9], quartz substrates [10], etc.), thick oxide films have advantages in terms of compatibility with standard semiconductor technology processes and mechanical properties.

Though thermal oxide is the best choice, it is not a practical way to produce thick silicon dioxide layers using standard high temperature oxidation methods [11]. In fact, because of the limited diffusion rate, a very long time is required to obtain thick oxide layers (several hundreds of hours to grow 30 μm thick films). Chemical vapor deposition (CVD) techniques [12] can also be used to produce thick silicon dioxide films due to a high growth rate (about 5 h to grow 30 μm thick films). Despite the higher deposition rate, electrical and mechanical properties of deposited oxide films are worse with respect to the thermal oxidation. A different approach involves the conversion of a portion of a silicon substrate into porous silicon by means of a simple anodization process followed by thermal oxidation [13]. Due to its huge surface/volume ratio (about 500 m²/cm³), porous silicon is easily changed in silicon dioxide. However, the oxidation of porous silicon results in a porous dioxide layer. Very recently a new approach was proposed in [14], which is based on the oxidation and the refilling of narrow trenches obtained on silicon by deep reactive ion etching (DRIE).

In this paper an alternative low cost method for the growth of silicon dioxide layers with thickness of several tens of microns is reported. The process is based on the photoelectrochemical etching of silicon in HF electrolytes, a well known technique to produce regular silicon microstructures (macropores, microtrenches, micropillars, microspindles, microchannels, etc.) [15,16]. This technique is here exploited to create deep high aspect ratio regular trenches, which are then completely oxidized to obtain a thick silicon dioxide layer.

2. Fabrication process

Thick silicon dioxide layers were produced by: (1) electrochemical formation of regular trenches with high aspect ratio and (2) full thermal oxidation of remaining silicon walls.
The fabrication process is schematically shown in Fig. 1. The starting material was an n-doped silicon wafer, (100) oriented, 2.4–4 $\Omega \cdot \text{cm}$ resistivity, 550 $\mu\text{m}$ thick. A silicon dioxide layer (5000 Å thick) was thermally grown on the sample (Fig. 1a). A standard photolithographic process was used for pattern definition. Straight lines, 2 mm in length and with different width and pitch were defined on the same sample. The size of the single pattern was about 2 mm$^2$. A BHF etch was then used to transfer the pattern to the silicon dioxide (Fig. 1b). Initial seeds for electrochemical etching were formed by KOH etching through the patterned silicon dioxide (Fig. 1c). The KOH etch time was long enough to obtain full V-grooves. Electrochemical etching in HF was then used to fabricate deep regular trenches in the patterned substrate, as detailed in the next section (Fig. 1d). The KOH etch time was long enough to obtain full V-grooves. Electrochemical etching in HF was then used to fabricate deep regular trenches in the patterned substrate, as detailed in the next section (Fig. 1d). The samples were rinsed in deionized water and then dried in a convection oven at 95$^\circ\text{C}$ for 10 min. The last step was a steam thermal oxidation performed at 1050 $^\circ\text{C}$. The oxidation time was long enough to completely convert the silicon to silicon dioxide, so obtaining a thick silicon dioxide layer (Fig. 1e and 1f). The samples were finally cleaved to allow scanning electron microscope (SEM) observation of the cross-sections.

The experimental setup used for photoelectrochemical silicon etching was constituted by an electrochemical cell made of polytetrafluoroethylene (PTFE) having a volume of 400 cm$^3$. The front side of the silicon sample was in contact with the electrolyte solution. The electrolyte composition was 1:2.17 (vol.) HF (48%):C$_2$H$_5$OH (99.9%):H$_2$O. Ethanol was added to reduce hydrogen bubbles formation at the sample surface, a commonly used technique for microporous silicon formation. For the same reason, the solution was stirred during the anodization process. The area of the sample exposed to the electrolyte solution was about 0.6 cm$^2$ and had a circular shape. Back side illumination of the sample was performed with a 300 W halogen lamp, positioned about 20 cm apart from the sample, through a circular window in the metal foil used to provide the electrical contact to the sample. The power supply of the lamp can be varied to modulate the etching photocurrent. The counter electrode was a platinum wire immersed into the electrolyte, close to the sample surface (about 5 mm). An HP4145B parameter analyzer was used to apply the anodization voltage and to monitor the etching current. All the experiments were performed at room temperature.

### 3. Experimental and results

The key role of the thick silicon dioxide formation process is played by the photoelectrochemical silicon etching for microtrench fabrication.

Electrochemical silicon etching in HF-based electrolytes is a well known technique to produce porous silicon [17]. Depending on the silicon doping, the type of the anodized substrate and the etching parameters, different pore morphologies can be obtained. Macroporous layers with micrometric regular straight pores can be obtained from illuminated n-type substrates (photoelectrochemical etching). By illuminating the back surface of the wafer with sufficiently energetic photons, holes can be generated in the substrate by a process of photon absorption. Under anodic biasing conditions, the photogenerated holes move to the front surface and silicon dissolution takes place. Initially, the electric field concentrates at sharp defects on the flat wafer surface. Surface defects therefore act as seeding points for macropore formation (Fig. 2a). As the etch progresses, the electric field still concentrates at the pore tips, where most of the injected holes reacts with the electrolyte so that a decreasing number of holes is then available for the dissolution of the side walls, that are therefore protected against dissolution (Fig. 2b).

By pre-patterning the wafer surface with defect sites it is possible to determine where macropores will grow (Fig. 2). KOH etching after a standard photolithographic step can be used to create inverse pyramidal notches in the required positions which can act as an array of defects. The macro pore morphology significantly depends on the anodization conditions, such as current density, etching time, HF concentration, temperature and bias, as well as on substrate properties, such as doping and orientation. Random [18] and pre-patterned [15] macropore arrays were grown on the
HF HF

(a) (b)

Fig. 2. Silicon macropore formation using electrochemical etching in HF solution.

same substrate through the wafer thickness [19] and on the whole surface of the wafer [20] with pores ranging from 2 to 15 μm [21]. Moreover, as demonstrated in a recent work [16], the macropore formation process can be employed as a micromachining technique for the fabrication of regular silicon microstructures with more complex geometries than the simple macropores array (for example, microwalls, microspirals, micropillars, microtubes, microtips, etc.).

In this work the electrochemical etching technique was used to produce microtrench arrays with different dimension and pitch on the same die. Three different line patterns were used as initial seeds for electrochemical etching: types, 1P2 (1 μm width lines with pitch of 2 μm); 2P4 (2 μm width lines with pitch of 4 μm); 4P8 (4 μm width lines with pitch of 8 μm). Dimension and pitch of lines were carefully chosen to comply with the oxidation step producing the thick silicon dioxide layer. In order to obtain thick oxide layers by means of trenches oxidation is necessary to make an area ratio (AR) (non-etched silicon to etched silicon area ratio) of about 0.8, so that a full oxidation of silicon walls results in trenches completely refilled by the grown oxide. The etching current was then properly tuned to obtain an AR of 0.8. A microtrench array of the type 2P4 is shown in Fig. 3. The trenches are about 30 μm deep corresponding to 20 min of etching time. We would like to outline that the depth of trenches is only limited by the etching time, so that trenches up to 100 μm or deeper can be obtained using this technique. Moreover, due to the fact that a negative feedback rules the electrochemical etching of silicon in HF solutions [19], it is easy to achieve high uniformity samples.

The oxidation time was targeted for structures of the type 2P4, having a better mechanical resistance with respect to the type 1P2 and a refilling time shorter than the type 4P8. We observed that three hours of wet oxidation were sufficient to completely convert the silicon to silicon dioxide and refill the trenches. In Fig. 4 such a sample is shown. It is clear that all the silicon was converted to silicon dioxide and a complete refill of trenches was at the same time obtained. The thickness of the produced oxide layer is about 30 μm, according to the depth of fabricated trenches.

We would like to outline that: (1) the thickness of the produced oxide layer only depends on the trenches depth so that layer up to 100 μm or thicker could be grown using deeper trenches; (2) furthermore, the oxidation time to completely convert the silicon to silicon dioxide only depends on the width (lateral thickness) of silicon walls so that the depth of trenches should not affect the oxidation time. This means that thicker oxide films could be obtained using the same oxidation time (3 h), only changing the trenches depth. Oxide thickness/fabrication time ratio greater than CVD methods could be then obtained with the proposed process.

HF HF

P opt P opt

Fig. 3. SEM cross-section of a silicon wall array (type 2P4) fabricated by means of the electrochemical etching in HF electrolyte.
Moreover, as the grown oxide is a thermal oxide, we could expect better properties with respect to CVD films.

Although highly regular thick silicon dioxide layers can be obtained from the process described above, as is visible in Fig. 4 top some details need to be highlighted and discussed.

A bumpy behavior characterizes the top surface of the oxide layer (see Fig. 4 bottom a and b), consequently to the fabrication process so that a chemical and/or mechanical polishing step is necessary to have a smoother surface. Further, we would like to point out that some voids exist on the top surface because of a non perfect joining of the silicon dioxide outgrowing in the trenches (see Fig. 4 bottom a and b). This effect is however restricted to few microns from the top surface and could be eliminated by means of the same polishing step used for smoothing the top surface. In fact, it can be noted that the trenches were perfectly refilled far off the surface, so that no void exists in the core of the oxide layer. In paper [14] some voids were observed probably due as suggested by the authors to the bowing of the DRIE trench profile. In the present case the electrochemical etching produces no significant bowing so that no voids were detected and no further process adjustment was needed.
A different effect was observed faraway from the surface. It seems that crystalline silicon walls were somewhere non completely consumed by the oxidation process so leaving crystalline silicon blades in the oxide layer. As a matter of fact, darker lines are somewhere visible in the middle of a silicon wall in the SEM pictures of Fig. 4 (bottom c and d). This effect could be ascribed to a non perfect constant dimension of walls produced by means of the electrochemical process and/or a non constant oxidation rate of them. However, although the crystalline nature of the darker lines in Fig. 4 can not be ruled out, further investigations also need to confirm it. This effect was also observed in [14] and it was ascribed to non complete oxidation. In any case, a thin crystalline blade into the oxide layer could not affect the properties of the material for most applications.

Finally, as is visible in Fig. 4 (bottom c and d), silicon spikes exist at the silicon dioxide-silicon interface. In fact, due to the macro pore formation process, trenches have a round section at the bottom (see Fig. 3), so that a full oxidation of silicon walls results in a silicon tip, as is clear in the cross-sections of Fig. 4 (bottom c and d).

4. Conclusions

In this paper a simple and low cost method for the growth of thermal silicon dioxide films with thickness of several tens of microns was demonstrated. The process is based on the photoelectrochemical etching of silicon in HF solution. This technique was here used to etch deep high aspect ratio regular trenches which were then completely oxidized to obtain a thick silicon dioxide layer. A morphological characterization of produced films was here reported. Further work will be devoted to perform electrical and thermal characterizations as well as to produce larger area thick silicon dioxide films.

References


Biographies

Giuseppe Barillaro received his laurea degree in Electronic Engineering and his Ph.D. degree in Information Engineering from the University of Pisa, Italy, in 1998 and 2001, respectively. Since November 2001, he has a post-doc position at the Information Department of University of Pisa. His main research interests concern porous silicon applications and technologies, silicon micromachining, solid state sensors, microelectronic devices and technologies.

Andrea Nannini was born in 1942, La Spezia, Italy. He graduated in Physics at the University of Pisa in 1969. From 1969 to 1972, he was with Centro di Studio per Metodi e Dispositivi per Radiotrasmissioni (National Research Council of Italy) at Faculty of Engineering, University of Pisa. Since 1973 he has been with the Department of Information Engineering, University of Pisa where currently he is full professor of Electronic Technologies. His main research interests are in the fields of solid-state devices and micromachining.
Giovanni Pennelli received his graduation in Electronic Engineering in 1992 and his Ph.D. in 1996 from the University of Pisa. In 1997 he had a research assistant position in the University of Glasgow, doing growth by MBE and characterization of compound semiconductors. Since 2000 he is assistant professor in the University of Pisa. His main field of interest are electron beam lithography, nanofabrication and nanodevice characterization, and new materials for electronics.