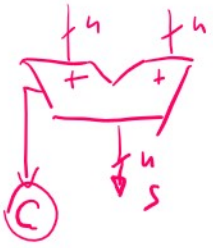
05_07_gio

giovedì 7 maggio 2020 07:35



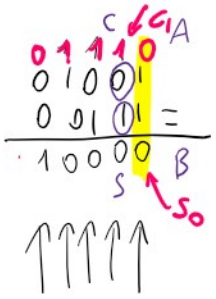
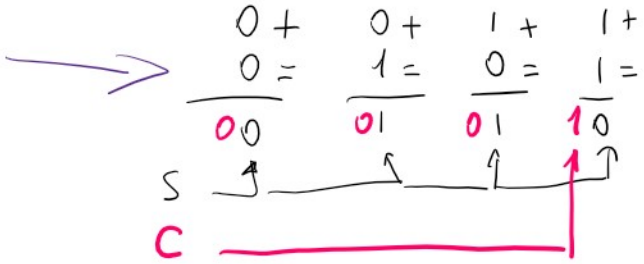


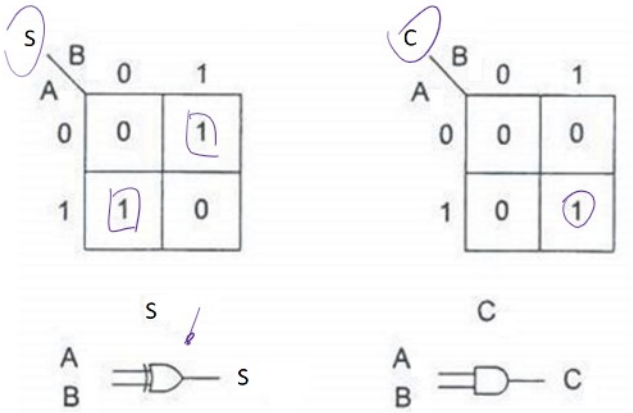
Tabella di verità del semi-sommatore (half adder)

IN OUT

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

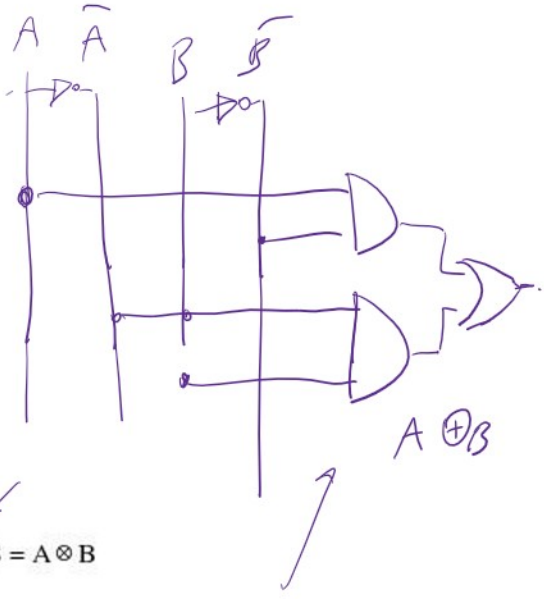
Tabella della verità del semisommatore





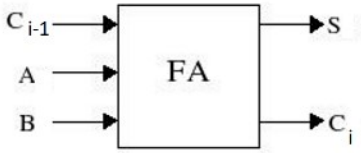
$\bar{A} \cdot B + A \cdot \bar{B}$

$A \oplus B$



Simbolo logico e realizzazione circuitale di un HA

Il sommatore completo
(full adder)



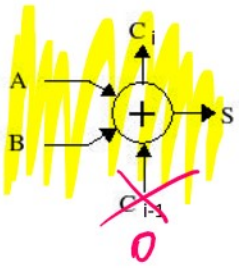
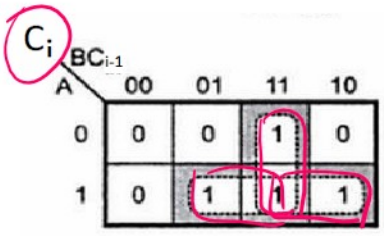


Tabella di verità del
sommatore completo a 1 bit
(full adder)

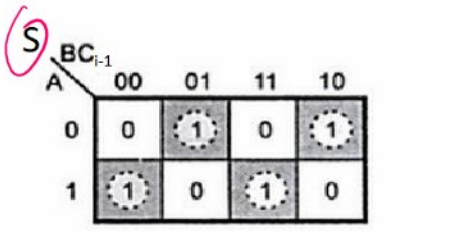
T.V. F.A.

A	B	C_{i-1}	S	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

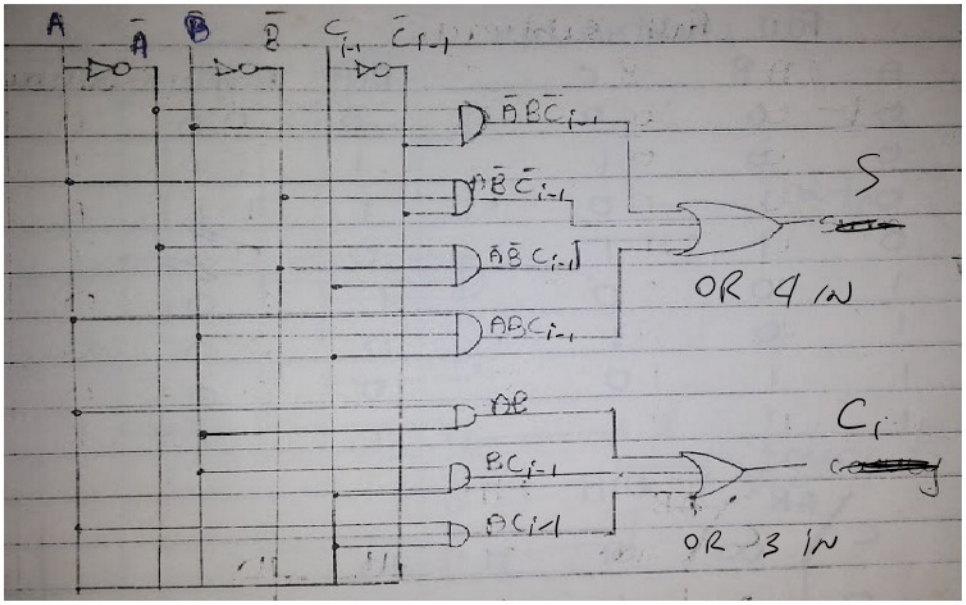
Tabella della verità del full adder



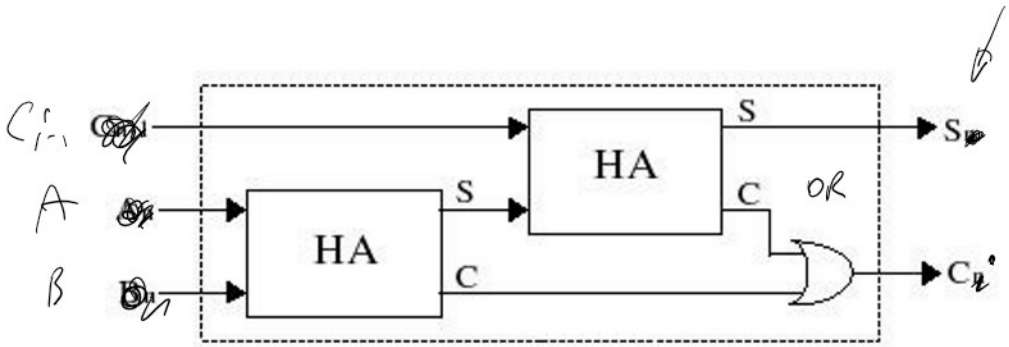
$C_i = AB + A C_{i-1} + B C_{i-1}$



$Sum = \overline{A}\,\overline{B}C_{i-1} + \overline{A}B\overline{C}_{i-1} + A\overline{B}\,\overline{C}_{i-1} + ABC_{i-1}$



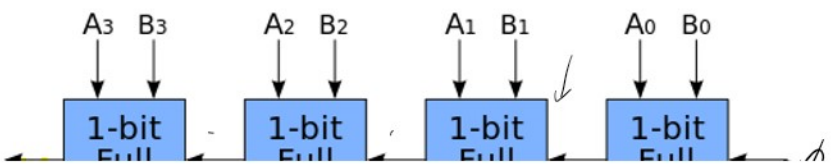
Sintesi del sommatore completo a 1 bit mediante due semi- sommatori ad 1 bit ed una porta OR

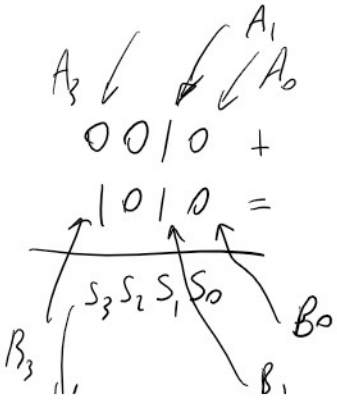


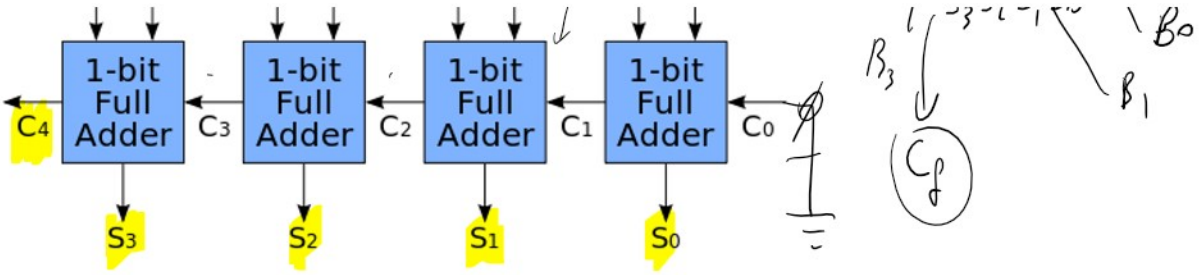
F. A.

Sommatore completo ad n bit, sintetizzato mediante n sommatori completi a 1 bit

F.A. a 4 bit





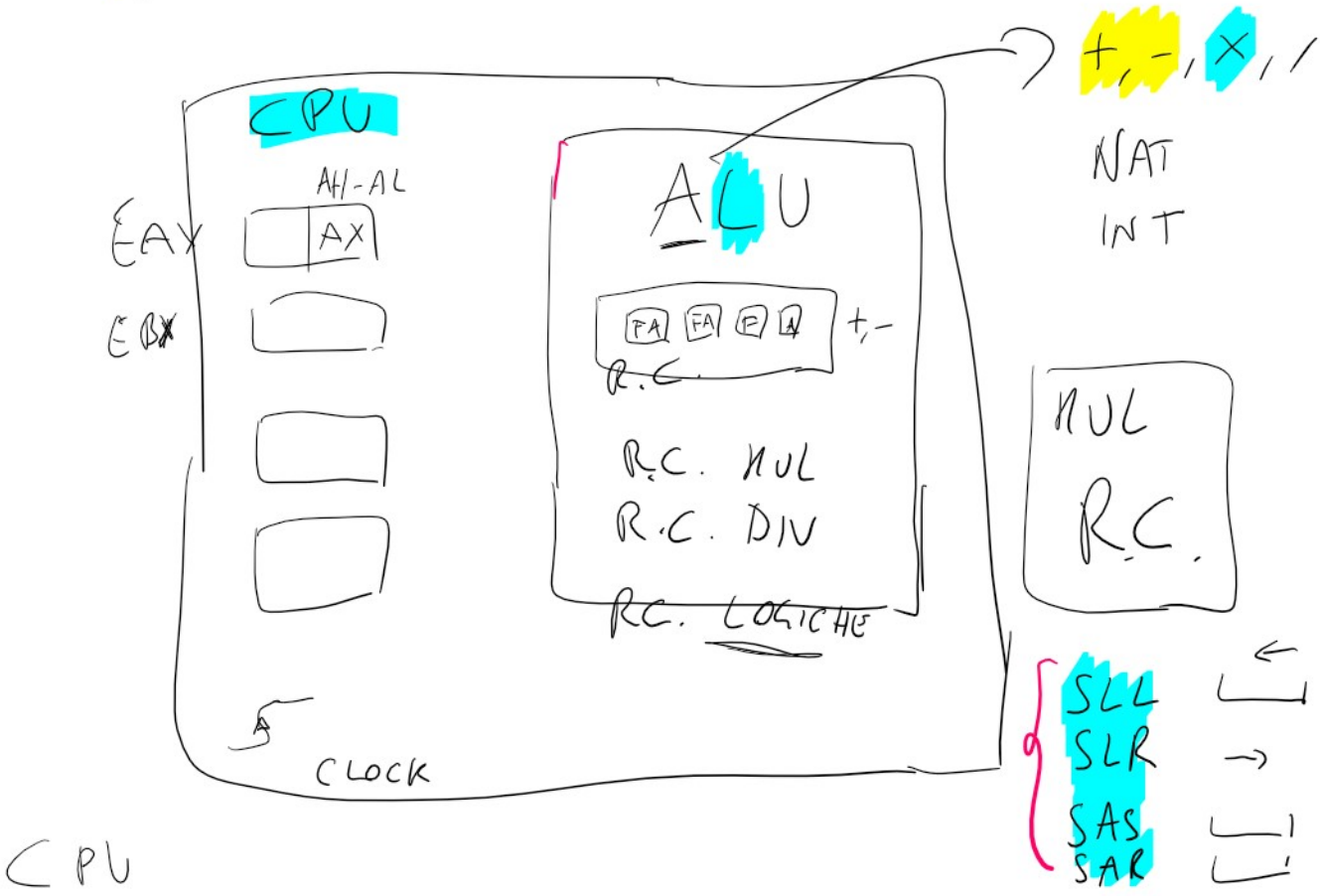


F. A. ad N-bit

8-bit ADD %BL, %AL (S, D) AL ← AL + BL

ADD %BX, %AX

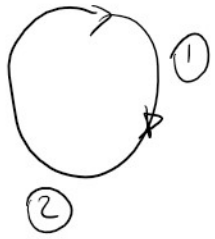
ADD %ECX, %EAX



1) Prelevare in memoria la prossima istr. da eseguire

/ [illegible] le prossime istr.
da eseguire

2) DECOD. e poi la si esegue



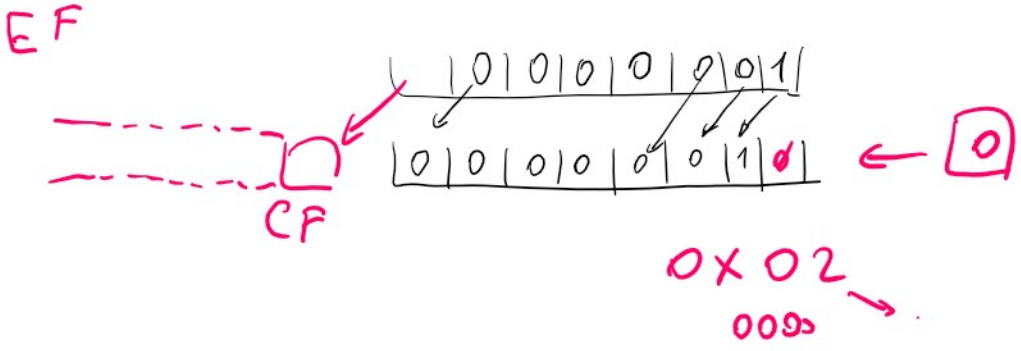
INC
DEC
ADD
MUL
DIV
IMUL
IDIV
SHL
SHR

⇒ var. comune

%AL

_main: mov $0b10000001, %AL

→ SHL $1, %AL → %AL
%EF



0x02
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